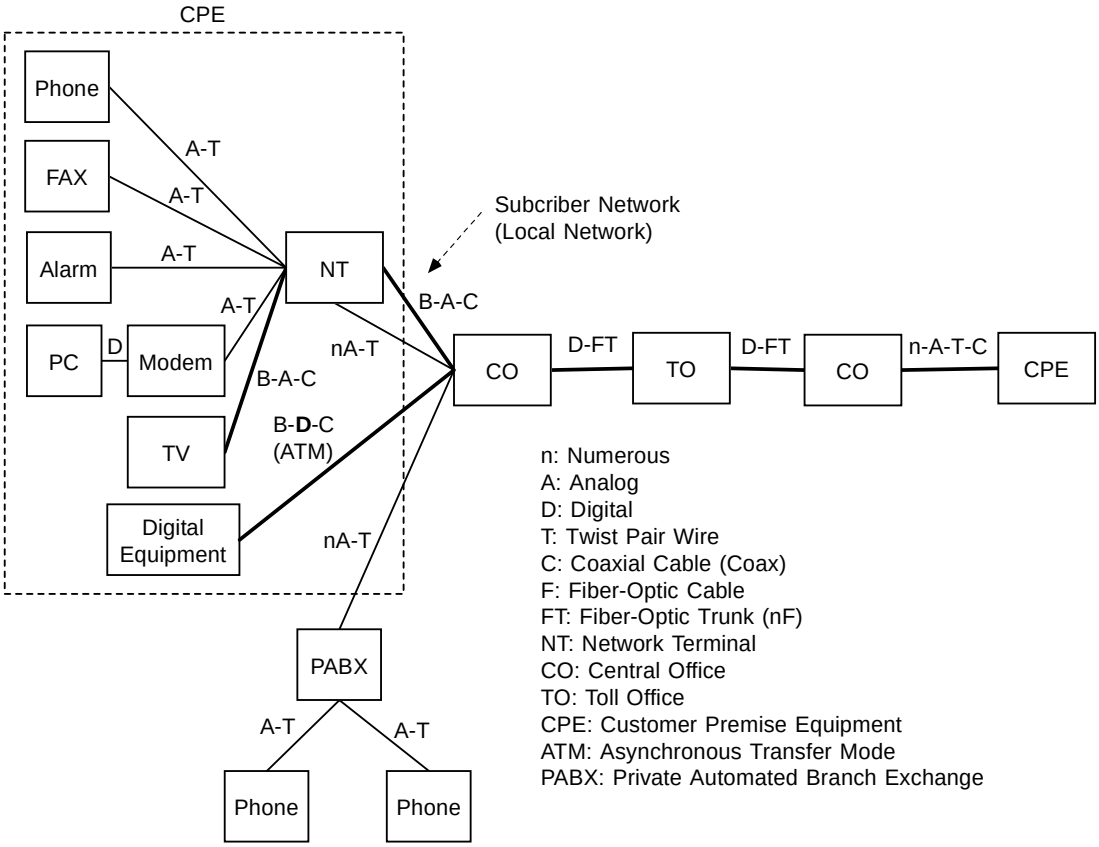
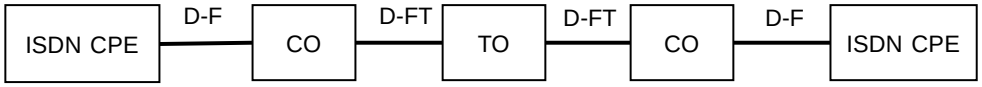
Digital Telephony

Duy-Ky Nguyen **9 Aug 97**

1. MODERN TELEPHONE NETWORK



FTTC (Fiber To The Curb)



ISDN Equipments are digital interface such as ISDN Phone, ISDN Modem, ISDN Terminal

FTTH (Fiber To The Home)

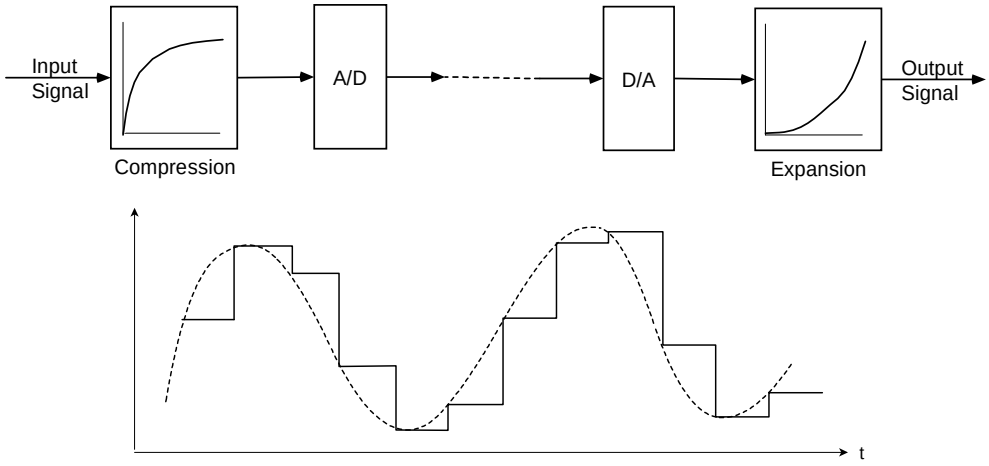
Fiber To The Curb: Fibers go to curbs only (outside home), they are terminated there, then twisted-pair wires / coaxial cables will continue going into home with analog / digital signals.

Fiber To The Home: Fibers go directly into home with all digital signals.

Transmission Media	Max Freq.	Max Length
Twist Pair Wire	Few Miles	Few Mbps
Coaxial Cable		
Fiber Optical Cable		

2. VOICE DIGITIZATION

An analog signal is digitized by PCM (Pulse Code Modulation) using a CODEC (Coder/Encoder). It is the zero-order hold in DSP with companding (compression at the transmitter and expansion at the receiver). This companding technique is required to improve the ratio of signal and noise. It use a nonlinear amplifier with higher gain for smaller signal since small signal is dominant in phone conversation.



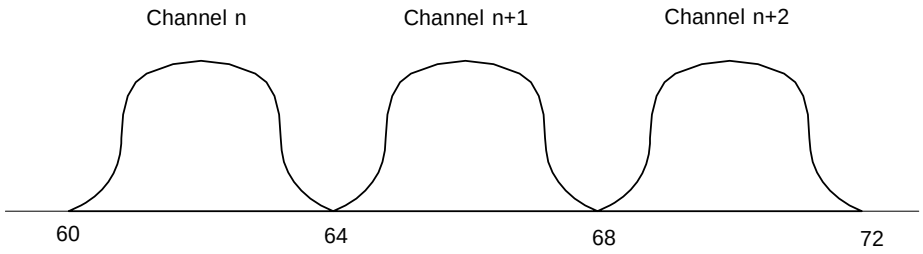
PCM (Pulse Code Modulation)

The normal voice band has an upper frequency bound of 3.5 KHz to 4 KHz, through the telephone network. This voice quality is not high, so it can be digitized with a resolution of 8 bits, *ie.* a sample is of 1 byte. To retain all of the information, sampling must be performed at twice the highest frequency contained in the signal being digitized. In this case, sampling must be performed at 8 KHz. Thus 8000 samples of 8 bits each, per second, is 64 Kbps. This is the digital bandwidth of the normal voice transmitted through the public telephone network.

3. MULTIPLEXING

3.1. Frequency Division Multiplex

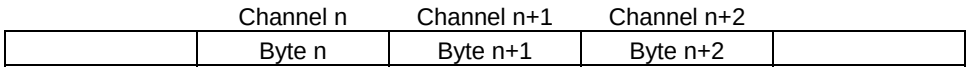
Frequency Division Multiplex is used to carry many channels on a phone line in an *analog* transmission since the bandwidth of each channel is 4 KHz enough voice and the bandwidth of the line is much higher, say 1 MHz then 250 channels. Each channel is at its own frequency range.



Frequency Division Multiplex (Analog Transmission)

3.2. Time Division Multiplex

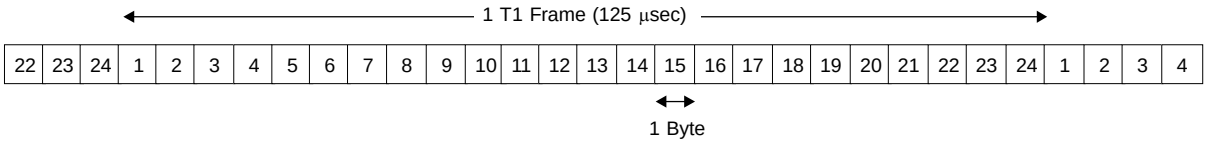
Time Division Multiplex is used to carry many channels on a phone line in a *digital* transmission since each channel is at its own *time slot.* A 4 KHz-bandwidth voice must be sampled at 8 KHz due to the Shannon Sampling Theorem, *ie.* 8000 samples/sec and thus 8 K x 8 = 64 Kbps if a sample corresponds to 1 byte (8 bits). If a channel accomodate 1 byte, then a 1 MHz-bandwidth line can transmit 1000/64 = 15.6 channels since 1 MHz equivalent to 1 Mbps in a (binary) digtal transmission. It seems that the digital transmission is less efficient than the analog one. However, the reverse is true since digital equipments is much cheaper and more reliable, this make the digital transmission even much cheaper as less equipments are required.



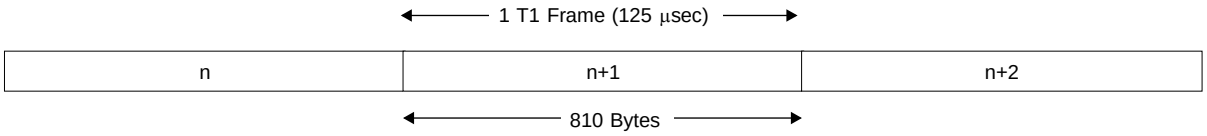
Time Division Multiplex (Digital Transmission)

There are 2 types of TDM:

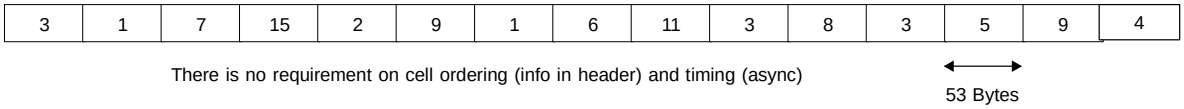
- Synchronous TDM in Telephony and SONET (*Synchronous* Optical Network) where data are sent in each frame at 8 KHz.
- Asynchronous TDM in ATM (*Asynchronous* Transfer Mode) where data are sent in each cell.



Digital Telephone Transmission



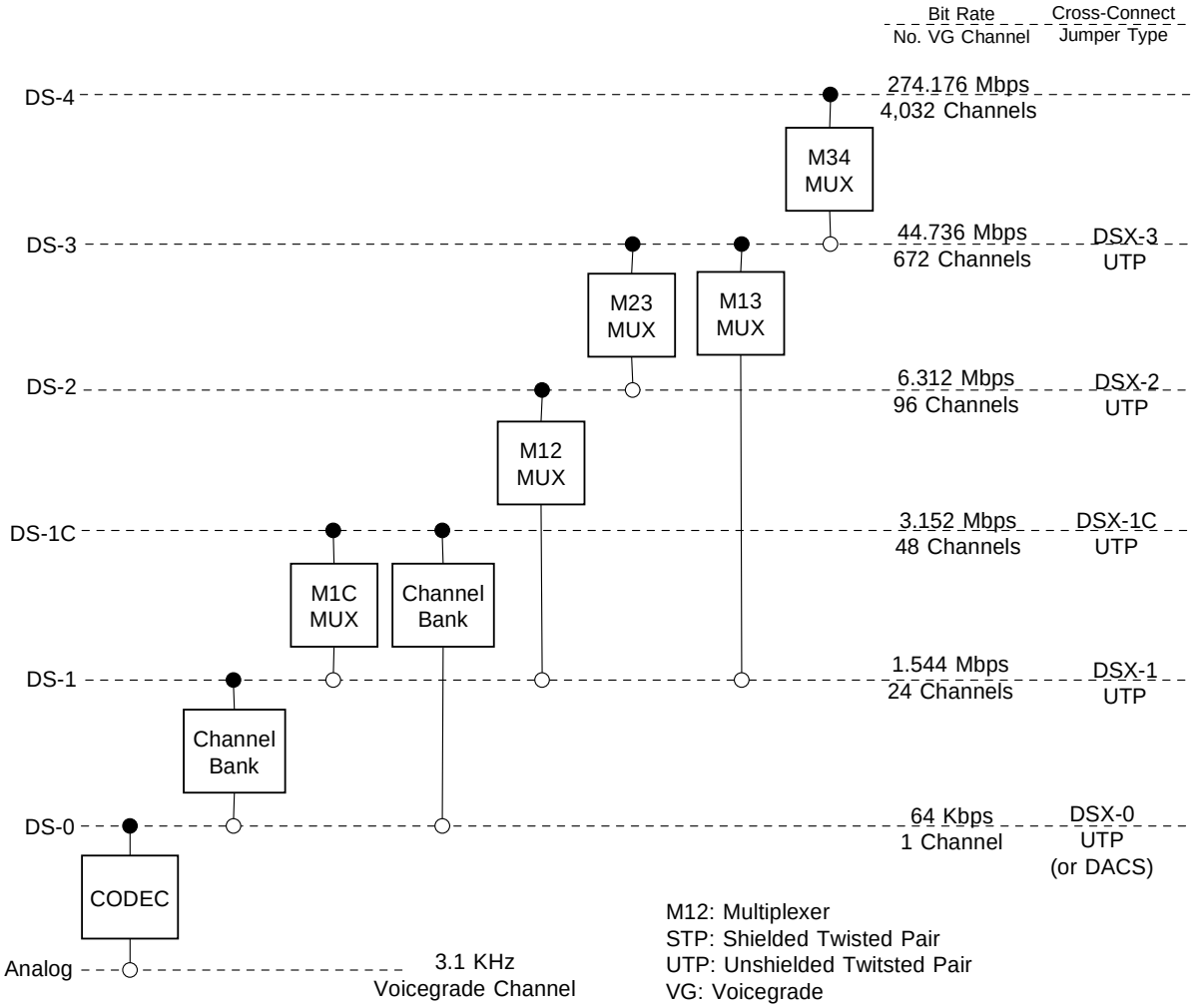
SONET Transmission



ATM Transmission

Digital TDM Signals of North America and Japan

Digital Signal Number	Number of Voice Circuits	Multiplex Designation	Bit Rate (Mbps)	Transmission Media
DS0	1	*Basic*	64 Kbps	T1 Paired Cable
DS1	24	D Channel Bank (24 analog inputs)	1.544	T1 Paired Cable
DS1C	48	M1C (2 DS1 inputs)	3.152	T1C Paired Cable
DS2	96	M13 (4 DS1 inputs)	6.312	T2 Paired cable
DS3	672	M13 (28 DS1 inputs)	44.736	Radio Fiber
DS4	4032	M34 (6 DS3 inputs)	274.176	T4M Coax WT4 Waveguide Radio



North America SONET Signal Hierarchy

Electrical Signal	Optical Signal	Data Rate (Mbps)
STS-1	OC-1	51.84
STS-3	OC-3	155.52
STS-9*	OC-9	466.56
STS-12*	OC-12	622.08
STS-18*	OC-18	933.12
STS-24*	OC-24	1244.16
STS-36*	OC-36	1866.24
STS-48*	OC-48	2488.32

* Not defined as Electrical standard

SONET Virtual Tributaries (VT)

Tributary Type	VT Designation	Payload Rate (Mbps)	Maximum Number in SPE
DS1	VT1.5	1.544	28
CEPT1	VT2.0	2.048	21
DS1C	VT3.0	3.152	14
DS2	VT6.0	6.312	7

3.3. Pulse Stuffing

The input digitals to subaggregate multiplexers are not always synchronized, nor need to be. Multiplexers use pulse stuffing (also called justification) techniques to synchronize several asynchronous or independent data streams. In this case, the aggregate digital stream has a higher rate than the sum of the individual channel rates to accommodate the extra pulses.

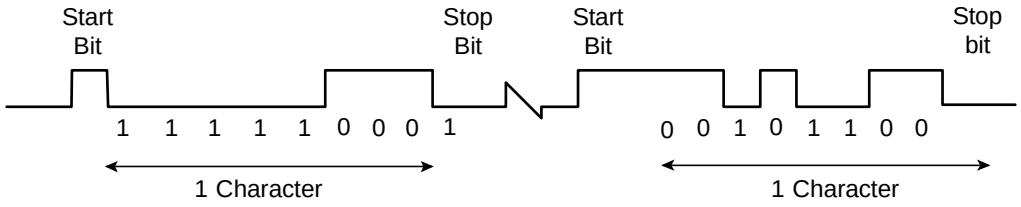
The digital hierarchy is based on multiplexers with bit stuffing capabilities at the DS-2, DS-3, and DS-4 rates. For example, the DS-2 rate consists of 4 DS-1 signals with a total rate of 6.176 Mbps (4 * 1.544 Mbps). Bit stuffing is used to raise the rate of each DS-1 to 1,545,796 bps. In addition to the DS-1 signals, the DS-2 rate includes 128,816 bps of overhead for alignment and bit stuffing control. This brings the aggregate to 6.312 Mbps (4 * 1,545,796 + 128,816). The aggregate is an even multiple of the 8 KHz sampling rate.

4. ASYNCHRONOUS VERSUS SYNCHRONOUS TRANSMISSION

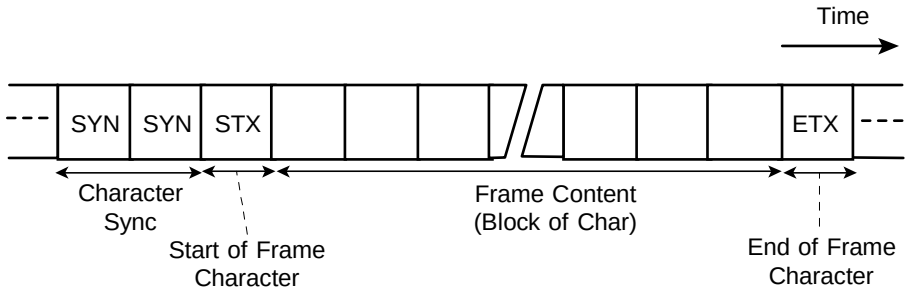
There are 2 basic modes of digital transmission involving 2 fundamentally different techniques for establishing a time base (sample clock) in the receiving terminal of a digital transmission link. The first of these techniques is *asynchronous* transmission, which involves separate transmissions of blocks of bits, normally *characters* of 8 bits each. Within an individual block a specific *predefined* time interval is used for each discrete signal. However, the transmission times of the blocks are unrelated to each other. Thus the sample clock in the receiving terminal is reestablished for reception of each block. With the second technique, called *synchronous* transmission, digital signals are sent continuously at a constant rate. Hence the receiving terminal must established and maintain a sample clock that id synchronized to the incoming data for an indefinite period of time.

4.1. Asynchronous Transmission

Asynchronous transmissions are used between computers via serial ports with RS232. Between transmissions an asynchronous line is in an inactive or idle state. The beginning of each transmission block is signified by a start bit and ended by stop bit(s). An asynchronous transmission automatically provides character framing. Since the very use of the term "asynchronous" implies a free-running clock in the receiver at a nominal rate, a certain amount of drift is inevitable in an asynchronous systems. The maximum length of each symbol block or character is determined by the limits of the initial phase inaccuracies and the maximum expected frequency difference between the transmitter and receiver clocks.



Asynchronous Serial Communication



Synchronous Serial Communication

4.2. Synchronous Transmission

Synchronous transmissions are exclusively used on the telephone network. Thus the line coding format for these systems must incorporate special considerations to ensure that each receiver can synchronize a local sample clock to the incoming signalling rate. Generally speaking, the synchronization requirements imply that a certain minimum density of signal transitions is required to provide continuous indication of signalling boundaries. Following are descriptions of 5 techniques for ensuring the existence of signal transitions for timing recovery:

1. Source code restriction
2. Dedicated timing bits
3. Bit insertion
4. Data scrambling

4.2.1. Source Code Restriction

All-zeros code word are precluded since there are no transitions for zeros. In case of 8-bit PCM code words, the exclusion of a single code word represents a loss in transmission capacity of only 1/256, this is not much for voice.

4.2.2. Dedicated Timing Bits

As an alternative to excluding transition-free data patterns, the line itself can periodically insert transition bearing bits onto the data stream. These bits are inserted at regular intervals, independently of the source data, to ensure the existence of a minimum number of signal transitions. For example, in a channel of 1 byte, only 7 bits are available to the user, the 8-th bit is reserved to provide an assurance that all 8 bits are not zero.

4.2.3. Bit Insertion

Another possibility for precluding unwanted line patterns id to use "bit insertion" *only* when necessary. For example, if 8 bits are all zero in a channel, then a one is inserted into the data stream. At the other end of the line, the one following 8 zeros is removed automatically.

4.2.4. Data Scrambling

Scrambling can be accomplished by adding a pseudorandom digital sequence to the transmitted stream, and then subtracting the same sequence from the received stream. In fact, modulo-2 operations are used due to binary data, thus addition and subtraction both become the mod-2 addition, *ie.* 1+1=0, 1+0=1, 0+0=0. This can be accomplished by the use of pseudorandom generators that are built alike, started in synchronism, and clocked at the same rate. The same random sequence is generated at both transmitter and receiver.

5. FRAMING

5.1. Super Frame (SF)

1 Frame = 24 Channels = 24 Bytes at 8 KHz

1 Super Frame = 12 Frames ⇒ 12 F-bit, 1 bit each Frame

Frame No.	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12
FAC bit (Odd)	1		0		1		0		1		0	
SAC bit (Even)		0		0		1		1		1		0
Composite Pattern	1	0	0	0	1	1	0	1	1	1	0	0
Signalling Frame (6n)						sa						sb

FAC (Frame Alignment Channel) is 101010.
SAC (Superframe Alignement Channel is 001110. To mark signalling frame, 0→1 for F6, 1→0 for F12.

All 8 bits of all channels are info except F6 and F12 (multiple of 6)
Every 8th bit of all 24 channel in F6 is sa-bit, thus only 7 bits info.
Every 8th bit of all 24 channel in F12 is sb-bit, thus only 7 bits info.
sa-bit and sb-bit create 4 states (idle, busy, ...).

5.2. Extended Super Frame (ESF)

1 Frame = 24 Channels = 24 Bytes at 8 KHz

1 Extended Super Frame = 24 Frames ⇒ 24 F-bit, 1 bit each Frame

Frame No.	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22	F23	F24
FAS Bit (4n)				0				0				1				0				1				1
C-Bit (2+4n)		c				c				c				c				c				c		
M-Bit (1+2n)	m		m		m		m		m		m		m		m		m		m		m		m	
Composite F-Bit	m1	c1	m2	f1	m3	c2	m4	f2	m5	c3	m6	f3	m7	c4	m8	f4	m9	c5	m10	f5	m11	c6	m12	f6
Signalling Frame (6n)						sa						sb						sc						sd

SF and ESF are not directly compatible on the same link.

The 24 F-bits are divided into 3 channels:

- Framing Pattern Sequence (FPS) as extended superframe alignment channel, f1 ~ f6. It is used to indicate boundary frame.
- Cycclic Redundancy Check (CRC, c1 ~ c6). It is used to monitor the performance of ESF.
- Data Link (DL, d1 ~ d12). It is used to send signals such as status signals, control signals, etc. Two signal format are used:
  * Bit-Oriented Signals (Repeat Bit Patterns)
  * Message-Oriented Signals using a predefined protocol.

All 8 bits of all channels are info except F6, F12, F18 and F24 (multiple of 6).
Every 8th bit of all 24 channel in F6 is sa-bit, thus only 7 bits info.
Every 8th bit of all 24 channel in F12 is sb-bit, thus only 7 bits info.
Every 8th bit of all 24 channel in F18 is sc-bit, thus only 7 bits info.
Every 8th bit of all 24 channel in F24 is sd-bit, thus only 7 bits info.
sa-bit, sb-bit, sc-bit and sd-bit create 16 states (idle, busy, ...).

5.3. SLC-96

SLC-96 (Subscriber Loo Carrier) is an extension of the SF and also known as TR8. The TR8 superframe consists of 72 frames of 193 bits each (1 F-bit and 24 channels of 8 bits each).

It has 72 F-bits, 36 FAC-bits (odd frame) are retained and have a repeating pattern of 1 0 1 0 . . .

The remaings are 36 SAC-bits form a DL to carry system status between the central office and remote terminal.

	Sync Word	Concentrator Field	Spoiler Field	Maintenance Field	Alarm Field	Protection Switch Field	Spoiler Field
No. of Bits (sum = 36)	12	11	3	3	2	4	1
Bit Position	1~12	13~23	24~26	27~29	30~31	32~35	36
Designation	SW	C1~C11	SP12~SP14	M15~M17	A1~A2	P20~P23	SP24

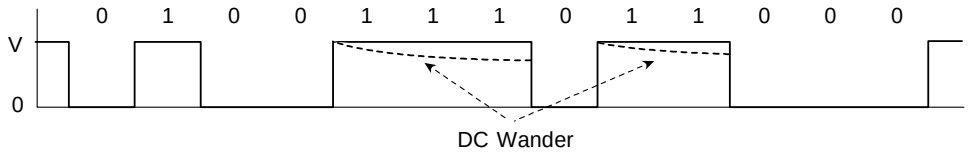
SW have a repeating pattern of 0 0 0 1 1 1 0 0 0 1 1 1 . . .
C1~C11 are used to assign channels dynamicaaly on a demand basis.
SP12~SP14, SP24=1 always, consist of the repeating pattern 0 1 0 . . ., which is used to prevent receiver misframing.
M15~M17 controls channel- and drop-side testing.
A1~A2 carriy alarm info and assiciated control commands.
P20~P22 controls switching of the protection kine.

6. LINE CODING

The return-to-zero (RZ) and nonreturn-to-zero (NRZ) are fundamental line codes upon which the line codes are based. An RZ line code uses pulses that have less than 100% duty cycle and therfore return to a zero voltage value before the next timeslot. An NRZ line code usually has 100% duty cycle, which means the voltage value is maintained throughout the pulse period.

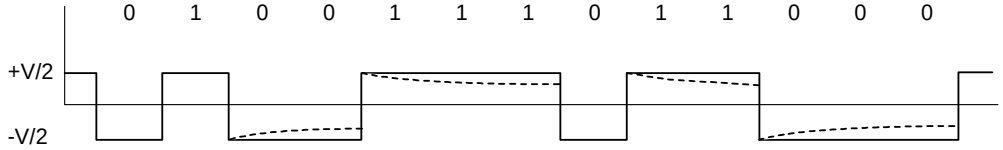
6.1. Unipolar Coding (RZ)

A unipolar code (RZ: Return-to-Zero) uses 0 v and *V* v for 0 and 1 of binary signal. A polar code, or NRZ (nonreturn-to-zero) code, uses -*V*/2 v and +*V*/2 v for 0 and 1 of binary signal. The latter technique consumes half power pf the former.



Unipolar Coding

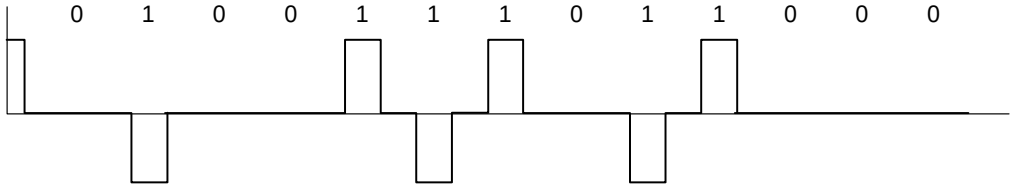
6.2. Polar Coding (NRZ)



Polar Coding

6.3. Bipolar Coding (AMI)

A limitation of level coding technique is a problem of DC wander. A bipolar coding uses 0 v for of signal 0 and alternate $\pm V$ v for signal 1. It is also referred to as "alternate mark inversion" (AMI). Since pulses on the line are supposed to alternate in polarity, the detection of 2 successive pulses of one polarity implies an error. This error condition is known as a "bipolar violation".



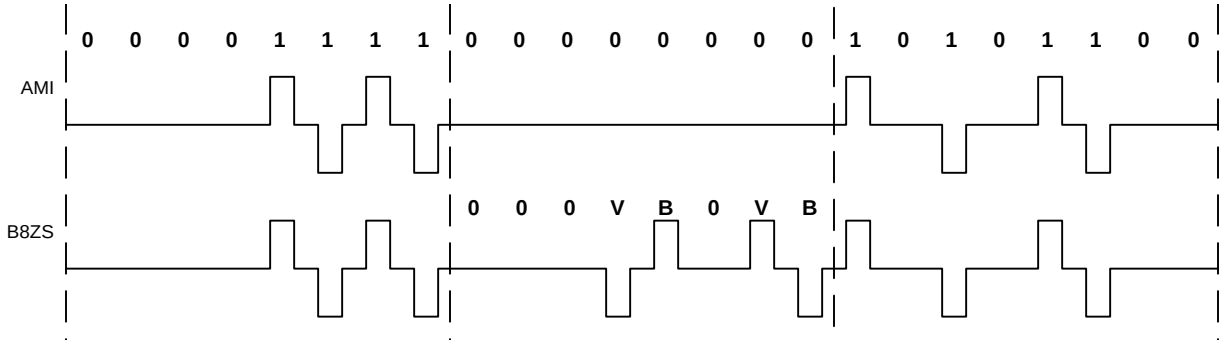
Bipolar Coding

6.4. Bipolar *N* Zero Substitution (B*N*ZS)

A major limitation of bipolar (AMI) coding is its dependence on a minimum density of 1's in the source code to maintain timing at the receiver. A low density of pulses on the line increases timing jitter and therefore produces higher error rates. Binary *N* zero substitution (BNZS) augments a basic bipolar code by replacing all strings of *N* zeros with a special *N* length code containing several pulses that purposely produce bipolar violations. In the B3ZS format, each string of 3 zeros in the source data is encoded woth either 00V or B0V (B: Bipolar, V: Violation, 0: No Pulse). If an odd number of 1's has been transmitted since the last substitution, 00V is chosen to peplace 3 0's. Otherwise, if an even number, B0V is chosen.

B8ZS Substitution Rules

Polarity of Preceding Pulse	Substitution
–	000–+0+–
+	000+–0–+
00000000	**000VB0VB**



HDB3 Substitution Rules

	Number of Bipolar Pulses (1's) since Last Substitution	
Polarity of Preceding Pulse	**Odd**	**Even**
–	00–	+00+
+	000+	–00–
	000V	**B00V**

7. 7. TRANSMISSION MONITORING

7.1. Framing Errors

The superframe format (SF) used with repeaterd T1-carrier has no inherent performance monitoring method, but limited error detection still is possible. The SF uses a framing abit followed by 192 data bits. The framing bit sequence takes on a fixed pattern, so once synchronization has been achieved, errors in the received frame pattern are easy to detect. However, of the 193 total bits transmitted in a frame, only one erroneous bit is detectable with absolute confidence; therfore, the error detection accuraacy is only (1/193 =) 0.52%, at best. The ESF uses a similar framing and framing error detection mechanism, but the ESF also has inherent error detection through the cyclic redundancy check (CRC) code.

When the frame pattern is lost, an out-of-frame (OOF) event has occurred. Generally, an OOF condition is declared when the terminal or network equipment senses errors in any 2-of-4, 2-of-5, or 3-of-5 consecutive terminal framing (F_t) bits. When an OOF event occurs, the framing mechanism may initiate a framing search. When the search reveals a difference in frame alignment, only then is aa change-of-frame alignment (COFA) made by choosing a new framing bit.

7.2. BPVs (Bipolar Violation)

Digital loop transmission systems follow specific line coding rules. When a line receiver detects a violation of these rules, a line code violation event has occurred. The AMI line code requires every pulse (binary one) to be transmitted with opposite polarity from the previous pulse. If 2 pulses in sequence are received with the same polarity, a BPV has occurred.

7.3. CRC Codes (Cyclic Redundancy Check)

We can associate an *m*-bit message of the form

11000001101100110111110010101010 1

with an *r*-bit binary number as the remainder from the division of this message by a constant *r*-bit divisor.

In CRC, binary mod-2 operations are used as its simplicity speeds up the processing where no “carry number” is required in its addition and its subtraction is identical to its addition. In fact, both mod-2 addition and subtraction are binary XOR operation which can be easily implemented in hardware for high-speed operations. Recall that a division is composed of successive subtractions.

Operand #1	Operand #2	XOR
0	0	0
0	1	1
1	0	1
1	1	0

The transmitter can incorporate the *r*-bit CRC code in the *m*-bit message as a separate remainder to obtain a new (*r* + *m*)-bit message, and the receiver computes remainder of the received message and compare with the received remainder. The more effective way is to use the zero remainer technique.

$$Message = \left(Quotient \otimes Divisor\right) \oplus Remainder$$

Adding *Remainder* to both sides gives

$$Message \oplus Remainder = \left(Quotient \otimes Divisor\right) \oplus Remainder \oplus Remainder$$

so

$$Message \oplus Remainder = \left(Quotient \otimes Divisor\right) \;\Rightarrow\; \frac{Message \oplus Remainder}{Divisor} = Quotient$$

as $X \oplus X = 0$.

To conserve the information, the *m*-bit original message is right-padded with *r* zeros before added to *r*-bit remainder to obtain a new (*r* + *m*)-bit message for transmission.

7.4. Loss of Signal (LOS)

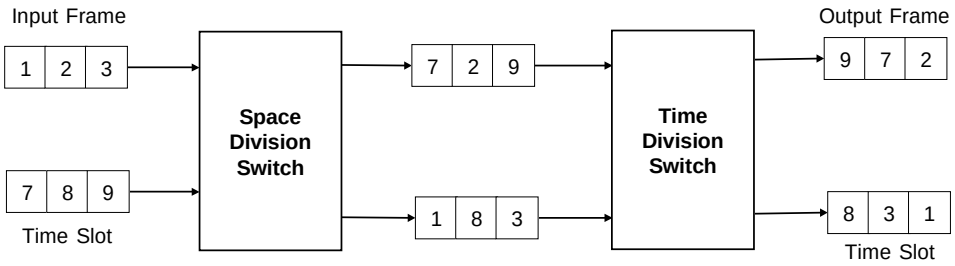
A LOS condition is declared when a receiver detects *N* (100, or 175, …) consecutive pulse positions with no pulses.

7.5. Alarms

Alarms give quick indications of performance problems. An alarm indication signal (**AIS**) is an all binary-ones signal (unframed) transmitted to maintain transmission continuity and to notify of an LOS or OOF. The AIS also id known as a **Blue alarm** and is used with both SF and ESF. The ITU G.704 framing format only has provisions for sending alarm cinditions to the other end by changing the S-bit in frame 12 from a binary zero to a binary one.

A **Red alarm** indicates a locally detected failure. It may be triggered either by a continuous or an intermittent LOS and LOF (Loss Of Frame) at the local terminal. A Red alrm in a local terminal will cause a **Yellow alarm** signal to be transmitted to the far-end. The colors (Red or Yellow) help to identify where the failure has occurred: Red, near; Yellow, far.

8. DIGITAL SWITCHING



Each channel is in a time slot, it can be changed to another line, but its order is unchanged

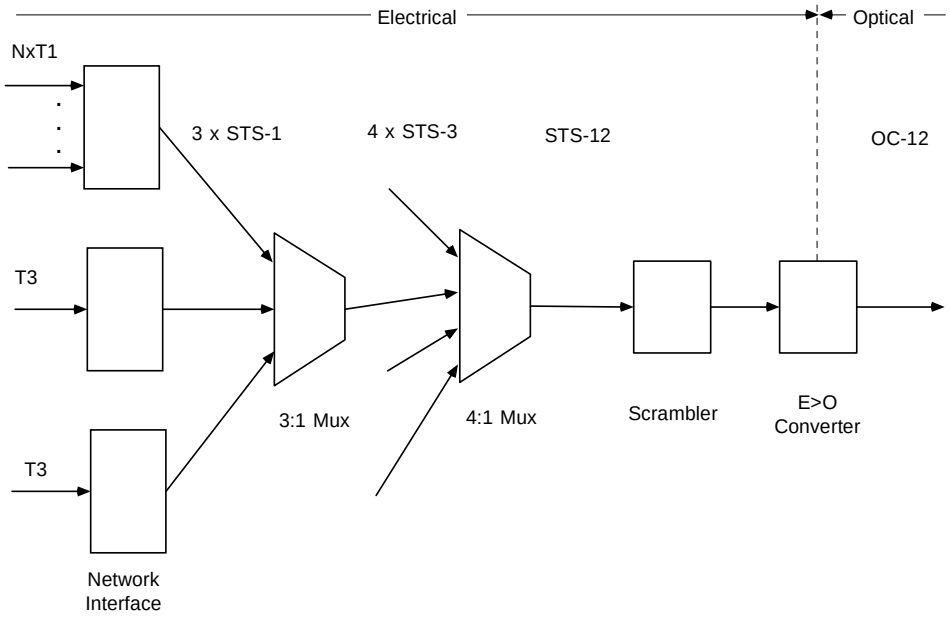
Order of Channel (Time Slot) is changed. Time Division Switch is composed of a Buffer, a Counter and a mapping Table (lookup)

9. SONET (SYNCHRONOUS OPTICAL NETWORK)

One frame of SONET has 810 bytes (9*90), thus the *basic* SONET channel STS-1 (Synchronous Transport Signal 1) is

$$810 * 8 * 8K = 51.84 Mbps$$

Since the bandwidth of fiber optics is very high, *N* STS-1 are multiplexed to have STS-*N*. Multiplexing is done byte for byte. For example, when 3 STS-1 tributaries (data stream to be merged) at 51.84 Mbps are merged into 1 STS-3 stream at 155.52 Mbps, the multiplexer first outputs 1 byte from tributary 1, then 1 from tributary 2, and finally 1 from tributary 3, before going back to 1.



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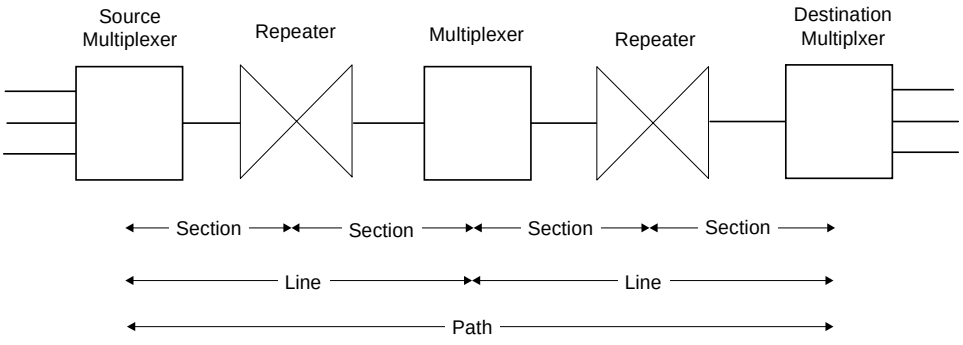
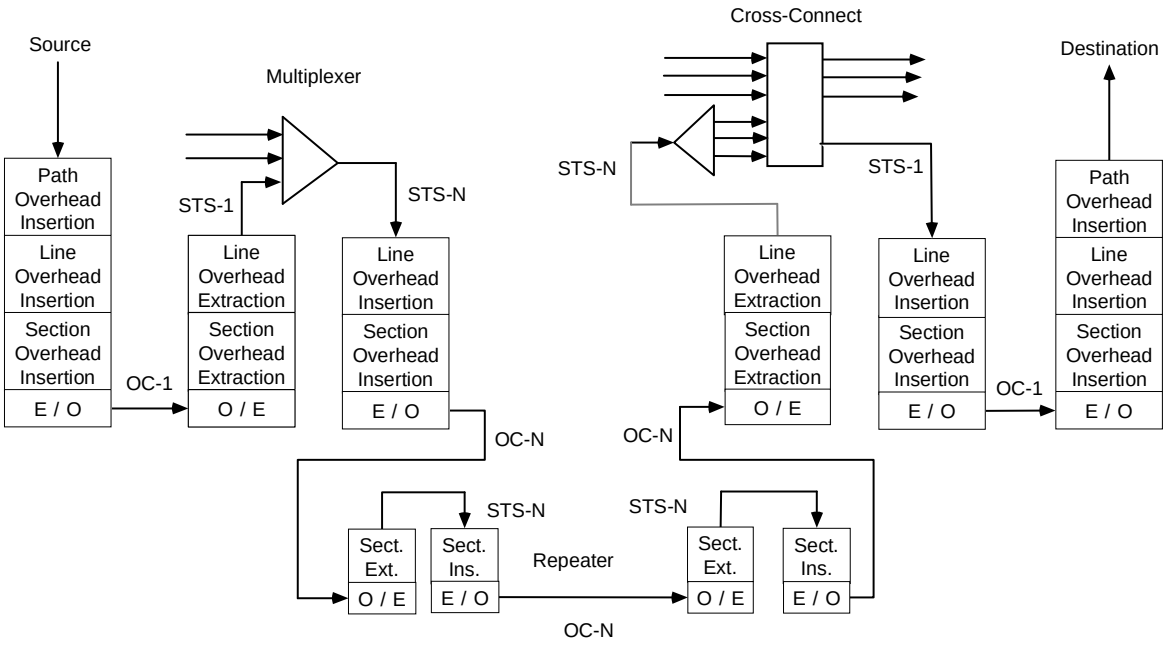
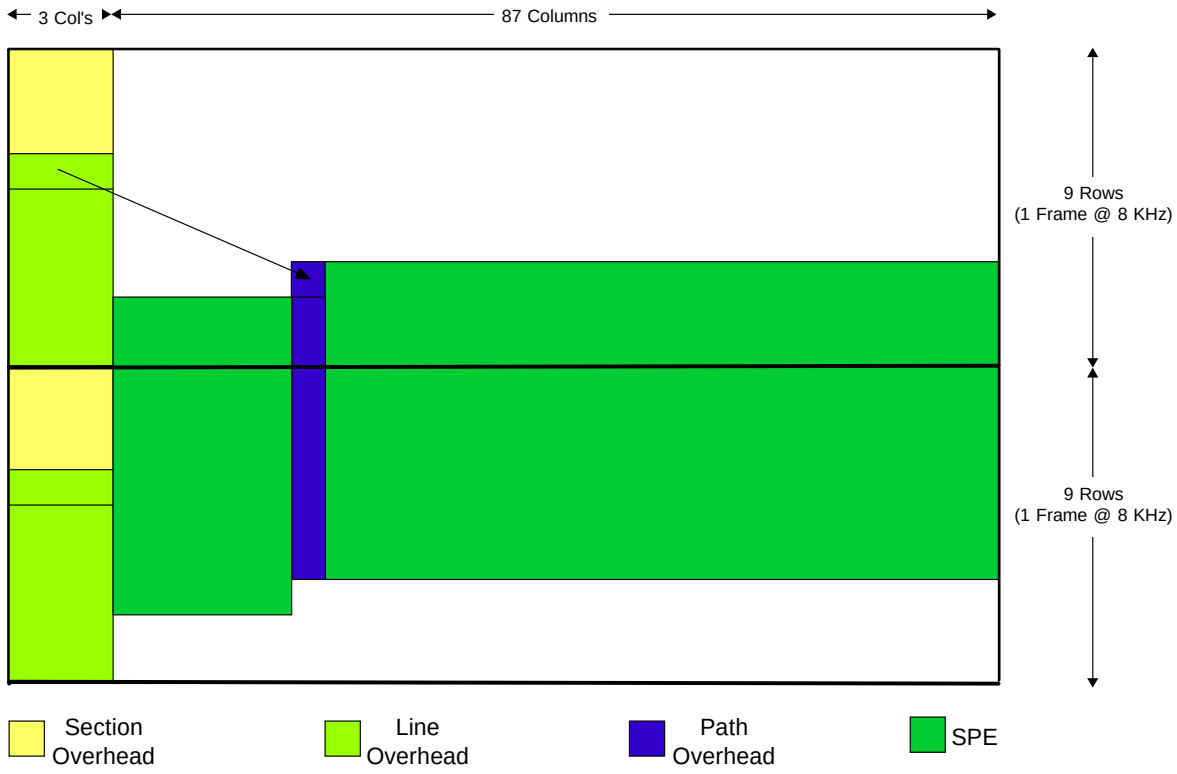
STS-24*	OC-24	1244.16
STS-36*	OC-36	1866.24
STS-48*	OC-48	2488.32

* Not defined as Electrical standard





The 810-byte SONET frame is best described as a rectangle of bytes, 9 rows by 90 columns.



Overheads are used for system Operation, Administration and Maintenance (OAM).

The ability to allow the user data SPE (Synchronous Payload Envelope) to begin anywhere within the SONET frame, and even to span 2 frame gives added flexibility to the system. For example, if a payload arrives at the source while a dummy SONET frame is being constructed, it can be inserted into the current frame, instead of being held until the start of the next one. This feature is also useful when the payload does not fit exactly on one frame, and in the case of a sequence of 53-byte ATM cells. The first row of the line overhead can then point to the start of the first full cell. to provide synchronization.

Section Overhead		
A1	A2	C1
B1	E1	F1
D1	D2	D3

A1~2: Framing Byte = F6, 28 hex (111 0110, 0010 1000)

C1: STS-1 ID identifies the STS-1 number (1 to N) for each STS-1 within an STS-N multiplex

B1: Bit-interleaved parity byte providing even parity over previous STS-N frame after scrambling

E1: Section level 64-kbps PCM orderwire (local orderwire)

F1: 64-kbps channel set aside for user purposes

D1~3: 192-kbps data communications channel for alarm, maintenance, control, and administration between sections.

Line Overhead		
H1	H2	H3
B2	K1	K2
D4	D5	D6
D7	D8	D9
D10	D11	D12
Z1	Z2	Z3

H1~3: Pointer bytes used in frame alignment and frequency adjustment of payload data; the functions of these bytes are defined.

B2: Bit-interleaved parity for line level error monitoring

K1~2: Two bytes allocated for signalling between kine level automatic protection switching equipment

D4~12: 576-kbps data communications channel for alarm, maintenance, control, and administration at the line level

Z1~2: Reserved for future use

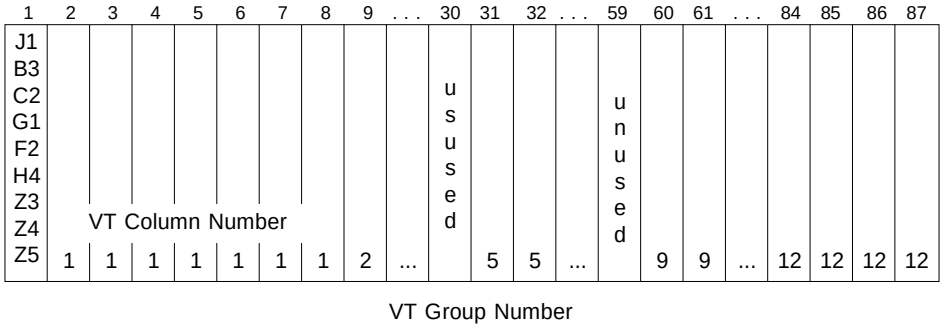
E2: 64 kbps PCM voice channel for kine level orderwire.

Path Overhead	Description
J1	64-kbps channel used to repetitively send a 64-byte fixed-length string so a receiving terminal can continuously verify the integrity of a path; the contents of the message are user programmable
B3	Bit-interleaved parity at the path level
C2	STS path signal label to designate equipped versus unequipped STS signals and, for equipped signals, the specific STS payload mapping that might be needed in receiving terminals to interpret the payloads
G1	Status byte sent from path terminating equipment back to path originating equipment to convey status of terminating equipment and path error performance (received BIP error counts)
F2	64-kbps channel for path user
H4	Multiframe indicator for payloads needing frames that are longer than a single STS frame; multiframe indicators are used when packing lower rate channels (virtual tributaries) into the SPE
Z3~5	Reserved for future use

Virtual Tributaries

To facilitate the transport of lower rate digital signals, the SONET standard used sub-STS-1 payload mappings referred to as virtual tributary (VT) structures. This mapping divides the SPE frame into 7 equal sized subframes or VT blocks with 12 columns (108 bytes) in each. Thus, the subframes account for 7*12 = 84 columns with the path overhead and 2 unused columns (reserved bytes R) accounting for the remainder of the 87 columns in the SPE.

In order to accommodate mixes of different VT types within an STS-1 SPE, the VTs are blocked together. An STS-1 SPE that is carrying Virtual Tributaries is divided into seven VT Blocks, with each VT Block using 12 columns of the STS-1 SPE; note that the number of columns in each of the different VT types -- 3, 4, 6, and 12 -- are all factors of 12. Each VT Block can contain only one size (type) of Virtual Tributary, but within an STS-1 SPE, there can be a mix of the different VT Blocks. For example, an STS-1 SPE may contain four VT1.5 blocks and three VT6 blocks, for a total of seven VT Blocks. Thus, an SPE can carry a mix of any of the seven blocks. The blocks have no overhead or pointers; they're just a way of organizing the different VTs within an STS-1 SPE.



- If a VT (VT block) has 12 columns, recall that each column has 9 rows (bytes), then
$$12 \times 9 \times 8 \times 8K = 6.912 \; Mbps$$

thus DS-2 of 6.312 Mbps is bit-stuffing to raise to this rate.This defines VT6.0 (6.312 ≈ 6.0 Mbps).

- If a VT (VT block) has 6 columns, recall that each column has 9 rows (bytes), then
$$6 \times 9 \times 8 \times 8K = 3.456 \; Mbps$$

thus DS-1C of 3.152 Mbps is bit-stuffing to raise to this rate.This defines VT3.0 (3.152 ≈ 3.0 Mbps).

- If a VT (VT block) has 4 columns, recall that each column has 9 rows (bytes), then
$$4 \times 9 \times 8 \times 8K = 2.304 \; Mbps$$

thus DS-0 of 1.544 Mbps is bit-stuffing to raise to this rate.This defines VT2 (2.304 ≈ 2 Mbps).

- If a VT (VT block) has 3 columns, recall that each column has 9 rows (bytes), then
$$3 \times 9 \times 8 \times 8K = 1.728 \; Mbps$$

thus DS-0 of 1.544 Mbps is bit-stuffing to raise to this rate.This defines VT1.5 (1.544 ≈ 1.5 Mbps).

SONET Virtual Tributaries

Tributary Type	VT Designation	Payload Rate (Mbps)	No. Columns per VT	Maximum Number in SPE
DS1	VT1.5	1.544	3	28 DS1
	VT2.0	2.304	4	
DS1C	VT3.0	3.152	6	14 DS1C
DS2	VT6.0	6.312	12	7 DS2

The 12 columns in a VT Block are not consecutive within the SPE; they're interleaved column by column with respect to the other VT blocks. As well, column 1 is used for the Path Overhead; the two columns of "fixed stuff" are assigned to columns 30 and 59.

The first VT Block, called Block 1, is found in every seventh column, starting with column 2, and skipping columns 30 and 59. That is, the 12 columns for VT Block 1 are columns 2, 9, 16, 23, 31, 38, 45, 52, 60, 67, 74, and 81.

Just as the VT Block columns are not placed in consecutive columns in an STS-1 SPE, the Virtual Tributary columns within a block are not placed in consecutive columns within that block. The columns of the individual VTs within the VT Block are interleaved as well. See Figure 14.

The VT structure is designed for transport and switching of sub-STS-1 rate payloads. There are four sizes of VTs: VT1.5 (1.728 Mb/s), VT2 (2.304 Mb/s), VT3 (3.456 Mb/s), and VT6 (6.912 Mb/s). In the 87 column by 9 row structure of the STS-1 SPE, these VTs occupy columns 3, 4, 6, and 12, respectively.

Two different modes of operation are defined for the VT structures: *locked and floating*. The *locked byte-synchronous mode* assigns every byte (DS0) of a tributary to a specific byte position in the SPE. If all 7 VTs are locked DS1s, all 672 DS0 channels (28 DS1 = 28 *24 DS0 = 672 DS0) are assigned to specific SPE time slots. In essence, this establishes a single-level digital signal with 672 channels. The locked mode of operation is the simplest interface to switching nodes but is inappropriate for interfacing to digital signals of the asynchronous hierarchy.

The *floating mode* of operation defines pointers to a VT-SPE payload in the same fashion as pointers to SPE payloads are defined at the STS-1 level. Thus, the floating VT-SPE mode allows for minimal framing delays at intermediate nodes and for frequency justification of VT-SPE undergoing transitions between timing boundaries. The floating mode has 2 different VT-SPE payload structures: *asynchronous multiplexing and byte-synchronous multiplexing*.

Table of VT1.5 Locations matched to the STS-1 SPE Column Numbers

VT Group #	VT #	Column #s
1	1	2,31,60
2	1	3,32,61
3	1	4,33,62
4	1	5,34,63
5	1	6,35,64
6	1	7,36,65
7	1	8,37,66
1	2	9,38,67
2	2	10,39,68
3	2	11,40,69
4	2	12,41,70
5	2	13,42,71
6	2	14,43,72
7	2	15,44,73
1	3	16,45,74
2	3	17,46,75
3	3	18,47,76
4	3	19,48,77
5	3	20,49,78
6	3	21,50,79
7	1	22,51,80
1	4	23,52,81
2	4	24,53,82
3	4	25,54,83
4	4	26,55,84
5	4	27,56,85
6	4	28,57,86
7	4	29,58,87

Column 1 = STS-1 POH
30 = Fixed Stuff
59 = Fixed Stuff

Asynchronous Multiplexing

The asynchronous operation is identical in concept to the bit-stuffing operation. The DS1 bit stream is inserted into the information bits (I) with no relationship to the VT-SPE frame or byte boundaries.

Because the asynchronous operation is compatible with the asynchronous network it is the format used in most SONET applications. The major advantage of the asynchronous mode of operations that it provides for totally transparent transmission of the tributary signal in terms of information and in terms of information rate. The major disadvantage of the asynchronous mode id that 64-kbps DS0 channels and signalling bits are not readily extracted.

Byte-Synchronous Multiplexing

In contrast to the asynchronous mode of operation, the byte-synchronous payload mappings allocate specific bytes of the payload to specific bytes (channels) of the tributary signals. Hence, this mode of operation overcomes the main drawback of the asynchronous mode in that 64-kbps channels and signalling bits within the payload are easily identified. In fact, the signalling bits of a DS1 are moved from the LSB of every 6-th frame of respective channels and placed in dedicated signalling bit positions within the VT-SPE. Thus byte-synchronous multiplexing offers an additional feature of converting from in-slot signalling to out-slot signalling for DS1 signals.

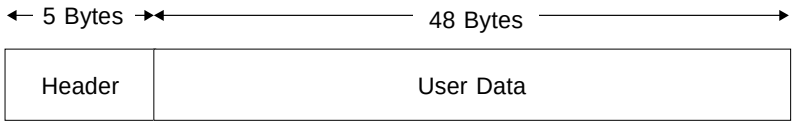
The major disadvantages of the byte-synchronous mode of operation are that transparency and timing adjustment capabilities are compromised. Transparency is diminished because the tributary signals must be channelized and contain framing to identify the channels. In contrast, the tributaries in the asynchronous mapping are merely bit streams (at 1.544 Mbps) with no specific internal structure required.

10. ATM (Asynchronous Transfer Mode)

A new wide area service is called B-ISDN (Broadband Integrated Services Digital Network) which will offer video on demand, live television from many sources, full motion multimedia electronic mail, CD-quality music, LAN interconnection, high-speed data transport for science and industry and many other services that have nt yet even been thought of, all over the telephone line.

The underlying technology that makes B-ISDN possible is called ATM (Asynchronous Transfer Mode) because it is not synchronous (tied to a master clock), as most long distance telephone lines are. Note that the acronym ATM here has nothing to do with the Automated Teller Machines many banks provide (although an ATM machine can use an ATM network to talk to its bank).

The basic idea behind ATM is to transmit all information in small, fixed-size packets called cells. The cells are 53 bytes long, of which 5 bytes are header and 48 bytes are payload.

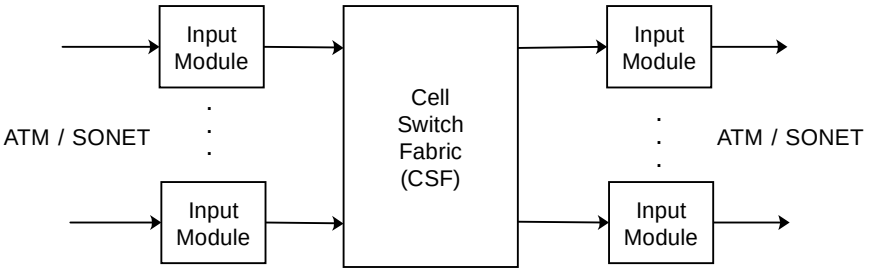


ATM has 2 types of interface correspoding to the 2 header formats below

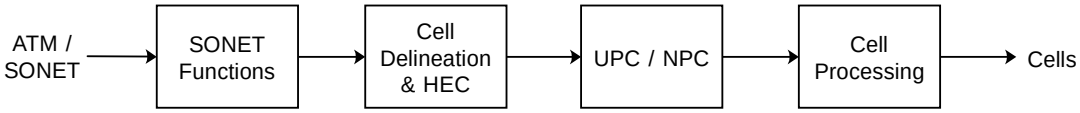
UNI (User-Network Interface)	GFC (4 bits)	VPI (1 Byte)	VCI (2 Bytes)	PTI (3 bits)	CLP	HEC (1 Byte)
UNI (Network-Network Interface)	VPI (1.5 Byte)		VCI (2 Bytes)	PTI (3 bits)	CLP	HEC (1 Byte)

GFC: General Flow Control
VPI: Virtual Path Identifier
VCI: Virtual Channel Identification
PTI: Payload Type
CLP: Cell Loss Priority
HEC: Header Error Check

ATM Switch Architecture



Input Module (IM)



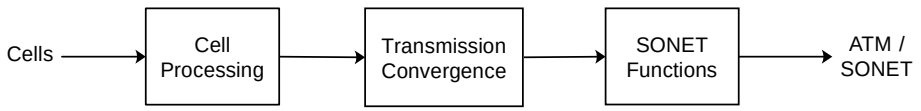
At each input port, the first function of an input module is termination of the incoming SONET signal extraction of the ATM cell stream. Basically, this involves:

- Conversion of the optical signal into an electrical one;
- Recovery of the digital bitstream;
- Processing of the SONET overhead;
- Cell delineation;
- Cell rate decoupling (discarding empty cells).

The cells must then be prepared for routing through the cell switch fabric. This requires a number of functions on each cell:

- Error checking in the cell header using the HEC field;
- Validation and translation of the VPI/VCI values;
- Determination of the destination output port;
- Usage/network parameter control for each VPC/VCC to be policed;
- Addition of an internal tag.

Output Module (OM)



The output modules perform many of the reverse functions of the input module. However, the OMs are considerably simpler than the IMs because their main responsibility is to prepare ATM cell stream for physical transmission. Specific function may include:

- Removal and processing of the internal tag from each cell;
- Possible translation of the VPI/VCI values;
- HEC field generation and inclusion into the cell headers;
- Cell rate decoupling (adding empty cells);
- Mapping cells into SONET payloads;
- Generation of SONET overhead;
- Conversion of the digital bitstream into an optical signal.

Cell Switch Fabric (CSF)

In general, the cell switch fabric is primarily responsible for transferring cells between the other functional; blocks in the switch. In particular, user data cells must be routed from the input modules to output modules.

Besides routing, a number of other possible functions of the cell switch fabric are important to consider:

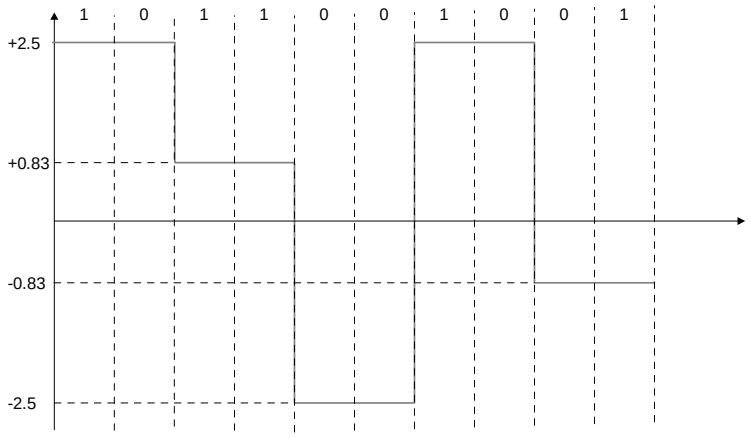
- Cell buffering;
- Traffic concentration and multiplexing;
- Multicasting or broadcasting;

11. xDSL (x Digital Subscriber Line)

Digital Subscriber Line

ISDN BRI (2B+D) is known as DSL or 2-wire 160 kbps where the payload is 2B + D = 2*64 + 16 = 144 kbps and the remaining is for CRC and M-bit. The line code 2B1Q is used to halve the bit rate (coding 2 bit at a time)

Sign Bit	Magnitude Bit	2B1Q
1	0	+3
1	1	+1
0	1	−1
0	0	−3



DSL (Digital Subscriber Line for ISDN-BRI 2B+D)	2-way 144-kbps Payload
HDSL (High-rate DSL for DS-1)	2-way 2x768 kbps Payload (Full Duplex)
ADSL (Asymmetric DSL for DS-1)	1-way 1.536 kbps (Simplex to User)