Clock Termination : Theory, Simulation and Verification

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1. Introduction

Back-plane design may appear as a trivial one, but it may not be quite right if clock termination is not fully appreciated. Improper termination results in ringing clock and hence unwanted multiplying frequency.

In control theory, ringing signal is due to an undamped case in linear systems with order higher than one. In transmission line, mismatched impedance will cause reflection and result ringing.

In this note, we'll find clock trace behaves as a loss-less transmission line and ringing clock is due to mismatched impedance. Note that clock trace is a copper wire, so it has zero Ohm resistance, hence a loss-less line. We start with transmission line theory to derive theoretical results used for MatLab simulations and then verifications using 3 real back-planes, say "A", "B" and "C". Lastly, there are some suggestions hopefully to improve clock quality in our products.

The interesting findings are (1) real verifications are consistent with theoretical simulations (2) via *may* have some effect on clock quality.

2. Transmission Line Theory

We say the line as has a series connection of inductance and resistance of l [*H/in*] and r [Ω/*in*] respectively and a parallel capacitance and conductance of c [*F/in* and g [*S/in*. Thus taking an infinitesimal segment of line, having length Δx, we have the model shown below

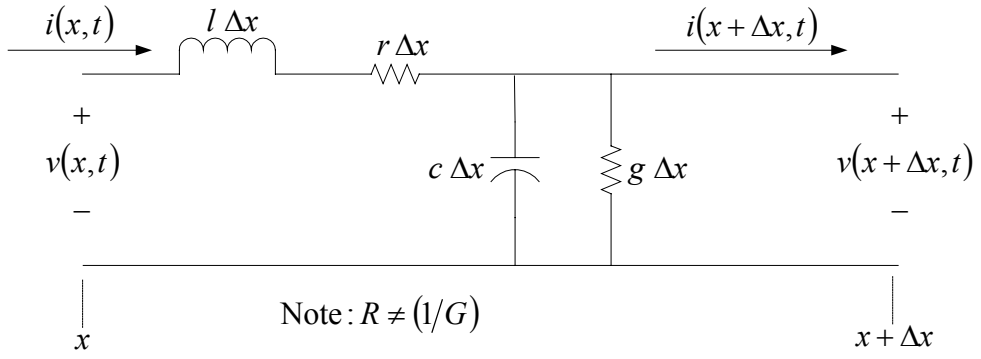


Fig.1 An infinitesimal strip of transmission line

We have

$$v(x,t) = (l\,\Delta x)\frac{\partial i(x,t)}{\partial t} + (r\,\Delta x)\,i(x,t) + v(x+\Delta x,t)$$

and

$$i(x,t) = (c\,\Delta x)\frac{\partial v(x+\Delta x,t)}{\partial t} + (g\,\Delta x)\,v(x+\Delta x,t) + i(x+\Delta x,t)$$

Thus collecting the terms with Δx we get as Δx approaches 0

$$-\left[l\frac{\partial i(x,t)}{\partial t} + r\,i(x,t)\right] = \lim_{\Delta x \to 0}\left[\frac{v(x+\Delta x,t) - v(x,t)}{\Delta x}\right] \equiv \frac{\partial v}{\partial x} \qquad (1)$$

$$-\left[c\frac{\partial v(x,t)}{\partial t}+g\,v(x,t)\right]=\lim_{\Delta x\to 0}\left[\frac{i(x+\Delta x,t)-i(x,t)}{\Delta x}\right]\equiv\frac{\partial i}{\partial x} \tag{2}$$

Now if we differentiate (1) with respect to x and (2) with respect to t we get

$$l\frac{\partial^2 i(x,t)}{\partial x\partial t}+r\frac{\partial i(x,t)}{\partial x}=-\frac{\partial^2 v(x,t)}{\partial x^2} \tag{3}$$

and

$$c\frac{\partial^2 v(x,t)}{\partial t^2}+g\frac{\partial v(x,t)}{\partial t}=-\frac{\partial^2 i(x,t)}{\partial t\partial x} \tag{4}$$

As $\partial^2/\partial x\partial t=\partial^2/\partial t\partial x$, substituting $\partial^2 i(x,t)/\partial t\partial x$ from(4) and $\partial i/\partial x$ from (2) into (3) to have

$$\frac{\partial^2 v(x,t)}{\partial x^2}=lc\frac{\partial^2 v(x,t)}{\partial t^2}+(gl+cr)\frac{\partial v(x,t)}{\partial t}+gr\,v(x,t) \tag{5}$$

Similarly,

$$\frac{\partial^2 i(x,t)}{\partial x^2}=lc\frac{\partial^2 i(x,t)}{\partial t^2}+(gl+cr)\frac{\partial i(x,t)}{\partial t}+gr\,i(x,t) \tag{6}$$

Equations (1), (2), (5), and (6) are called the Telegrapher's Equations.

If we assume zero initial conditions and take Laplace transforms, we reduce these partial differential equations to the *2nd* order ordinary homogeneous linear differential equations

$$\frac{d^2V(x,s)}{dx^2}=\left[lcs^2+(gl+cr)s+gr\right]V(x,s) \tag{7}$$

and

$$\frac{d^2I(x,s)}{dx^2}=\left[lcs^2+(gl+cr)s+gr\right]I(x,s) \tag{8}$$

These equations are easily solved, but the general case leads to rather complicated Laplace Transforms.

A clock trace on a PCB (Printed Circuit Board) behaves as a *lossless transmission line*, *i.e.*

$$r=g=0 \tag{9}$$

We shall restrict ourselves to this interesting special case. Then the solutions to (7) and (8)are

$$V(x,s)=Ae^{s\eta x}+Be^{-s\eta x} \tag{10}$$

and

$$I(x,s)=Ce^{s\eta x}+De^{-s\eta x} \tag{11}$$

where

$$\eta^2=lc \tag{12}$$

The constants are obtained by using the boundary conditions (see Fig. 2)

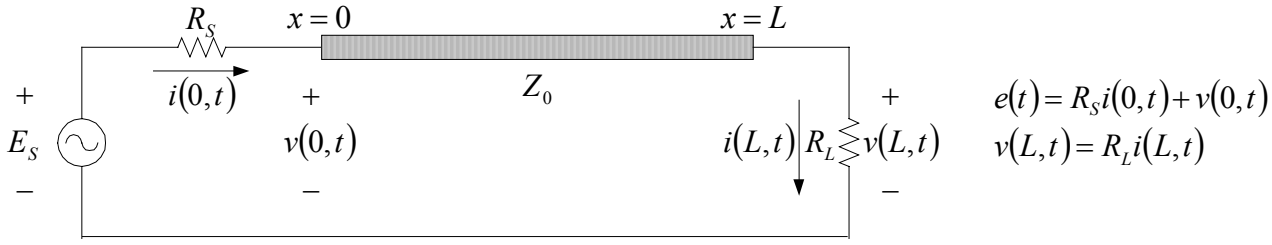


Fig.2 The Boundary Conditions

Using the boundary conditions implied by the Figure 2, with $g = 0$ in (2), we get

$$E(s)=V(0,s)+R_SI(0,s) \tag{13}$$

$$V(L.s)=R_LI(L,s) \tag{14}$$

and $$\frac{dI(x,s)}{dx} = -scV(x,s) \tag{15}$$

Applying (15) to (7) and (8) we have

$$s\left(\eta Ce^{s\eta x} - \eta De^{-s\eta x}\right) = -sc\left(Ae^{s\eta x} + Be^{-s\eta x}\right)$$

Since this is true for all x, so at at $x\to+\infty$, we have

$$\eta C = -cA \tag{16}$$

and at $x\to-\infty$

$$\eta D = cB \tag{17}$$

We now define $$Z_0 = \eta/c = \sqrt{l/c} \tag{18}$$

known as *characteristic impedance* and write $A = -Z_0 C$ and $B = Z_0 D$, then

(13) is $$E(s) = A + B + \left(-A + B\right)\left(R_S/Z_0\right) \tag{19}$$

and (14) is $$Ae^{s\eta L} + Be^{-s\eta L} = \left(-Ae^{s\eta L} + Be^{-s\eta L}\right)\left(R_L/Z_0\right) \tag{20}$$

Combining terms to get A & B :

$$Z_0 E(s) = A\left(Z_0 - R_S\right) + B\left(Z_0 + R_S\right) \tag{21}$$

and $$0 = Ae^{s\eta L}\left(Z_0 + R_L\right) + Be^{-s\eta L}\left(Z_0 - R_L\right) \tag{22}$$

Now we multiply (21) by $e^{s\eta L}\left(Z_0 + R_L\right)$ and (22) by $Z_0 - R_S$ to get

$$e^{s\eta L} Z_0\left(Z_0 + R_L\right)E(s) = Ae^{s\eta L}\left(Z_0 + R_L\right)\left(Z_0 - R_S\right) + Be^{s\eta L}\left(Z_0 + R_L\right)\left(Z_0 + R_S\right) \tag{23}$$

and $$0 = Ae^{s\eta L}\left(Z_0 + R_L\right)\left(Z_0 - R_S\right) + Be^{-s\eta L}\left(Z_0 - R_L\right)\left(Z_0 - R_S\right) \tag{24}$$

Substracting (23) to (24), we get

$$B = \frac{e^{s\eta L} Z_0\left(Z_0 + R_L\right)E(s)}{e^{s\eta L}\left(Z_0 + R_L\right)\left(Z_0 + R_S\right) - e^{-s\eta L}\left(Z_0 - R_L\right)\left(Z_0 - R_S\right)} \tag{25}$$

Dividing numerator and denominator by $\left(Z_0 + R_L\right)\left(Z_0 + R_S\right)$ to have

$$B = \frac{Z_0}{Z_0 + R_S}\frac{e^{s\eta L}E(s)}{e^{s\eta L} - \rho_S\rho_L e^{-s\eta L}} = \frac{Z_0}{Z_0 + R_S}\frac{E(s)}{1 - \rho_S\rho_L e^{-2s\eta L}} \tag{26}$$

where $$\rho_S = \frac{R_S - Z_0}{R_S + Z_0}, \qquad \rho_L = \frac{R_L - Z_0}{R_L + Z_0} \tag{27}$$

known as reflection coefficient at source and load, respectively

From (24) we then get

$$A = B\frac{e^{-s\eta L}\left(R_L - Z_0\right)}{e^{s\eta L}\left(R_L + Z_0\right)} = e^{-2s\eta L}\rho_L B \tag{28}$$

Thus $$V(x,s) = E(s)\left(\frac{Z_0}{Z_0 + R_S}\right)\left(\frac{e^{-s\eta x} + \rho_L e^{-s\eta(2L-x)}}{1 - \rho_S\rho_L e^{-2s\eta L}}\right) \tag{29}$$

We consider a 5-unit step response at the load $x=L$

$$V(L,s) = \frac{5}{s}\left(\frac{Z_0}{Z_0 + R_S}\right)\left(\frac{1 + \rho_L}{1 - \rho_S\rho_L e^{-2\eta Ls}}\right)e^{-\eta Ls} = \frac{5}{s}\left(\frac{2R_L}{R_L + Z_0}\right)\left(\frac{Z_0}{Z_0 + R_S}\right)\left(\frac{e^{-\eta Ls}}{1 - \rho_S\rho_L e^{-2\eta Ls}}\right) \tag{30}$$

as $$1 + \rho_L = 1 + \frac{R_L - Z_0}{R_L + Z_0} = \frac{2R_L}{R_L + Z_0}$$

where 5-unit step function is chosen to compare with clock of 5 V amplitude in verifications.

We'll study its time response using Laplace Transform and MatLab for matched and mismatched conditions in series and parallel termination lines.

3. MatLab Simulations

Each via on a clock trace behaves as a joint of 2 transmission lines and where reflections occur. That's why clock traces must not have via along the line. Via at load is OK as it's not on the transmission line. Unfortunately, on both back-planes of "A" and "B" back-planes, clock traces do have vias, the "B" back-planes has more! Clock traces in internal layer 5 has $Z_0 \approx 50\,\Omega$ and layer 6 has $Z_0 \approx 44\,\Omega$. We arbitrarily choose layer 5 with

$$l = 16.28 \;\; nH/in$$

and

$$c = 6.531 \;\; pF/in$$

thus its characteristic impedance is

$$Z_0 = 49.922\,\Omega$$

Typically, the load is roughly distant from the source by

$$L = 30 \;\; in$$

3.1. Matched Impedance

We have 2 cases

(1) Series Termination $R_S = Z_0, \quad R_L = \infty \;\; (open)$

(2) Parallel Termination $R_S = 0, \quad R_L = Z_0$

In both cases, Eq.(30) becomes

$$V(L,s) = \frac{5}{s} e^{-\eta L s}$$

then

$$v(L,t) = 5\,\mathcal{U}(t - \eta L)$$

where

$$\mathcal{U}(t - \eta L) = \begin{cases} 0 & if \;\; t < \eta L \\ 1 & if \;\; t \geq \eta L \end{cases} \qquad (31)$$

Its time response is ideal as it's identical to the input signal with some delay as seen in Fig.3

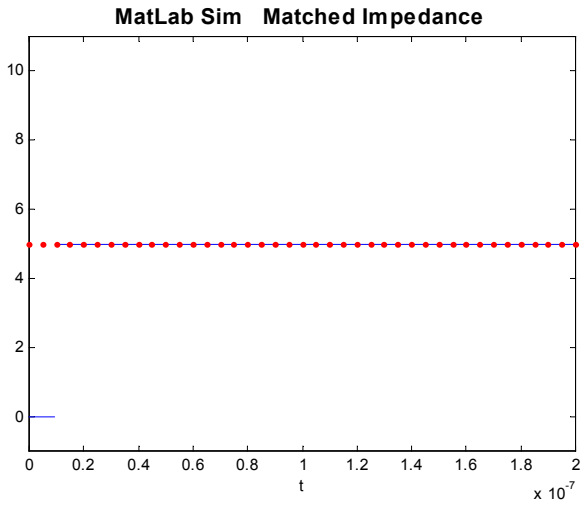


Fig.3 Matched Impedance

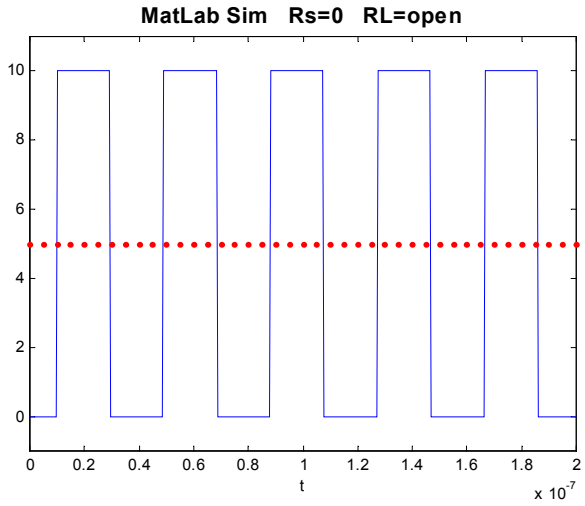


Fig.4 $R_s = 0$ R_L = open

3.2. Mis-Matched Impedance

If $$R_S = 0, \quad R_L = \infty \,(open)$$

then Eq.(30) becomes

$$V(L,s) = \frac{5}{s}\frac{1}{\cosh(\eta L s)}$$

thus $$v(L,t) = 5\left[1 + \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{(-1)^n}{2n-1}\cos\frac{(2n-1)\pi t}{2\eta L}\right]$$

Its time response is totally affected by full reflection to have a square wave of amplitude 10 V instead of 5V constant amplitude as seen in Fig.4!

If there's a load resistor, we have mismatched parallel termination as in Fig.5 and both mismatched series and parallel terminations as in Fig.6.

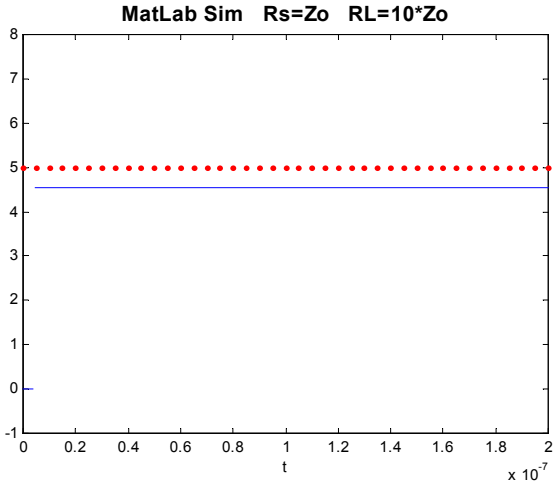


Fig.5 $R_S = Z_0 \quad R_L = 10Z_0$

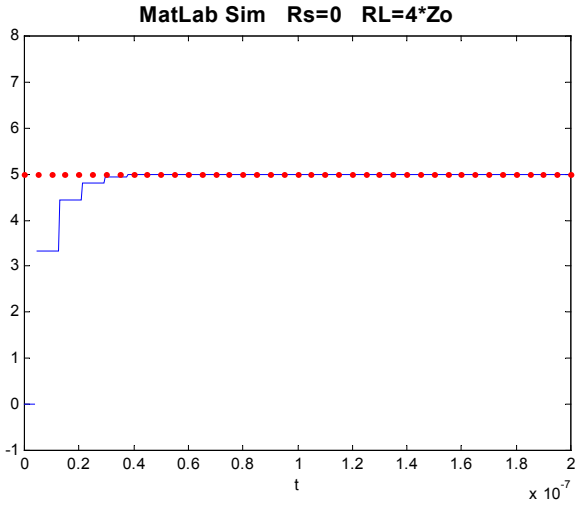


Fig.56 $R_S = 0 \quad R_L = 4Z_0$

If there's no load resistor, we have Fig.8

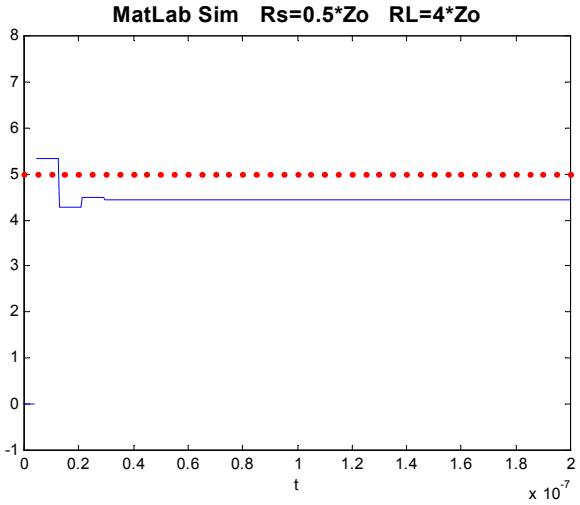


Fig.7 $R_S = 0.5Z_0 \quad R_L = 4Z_0$

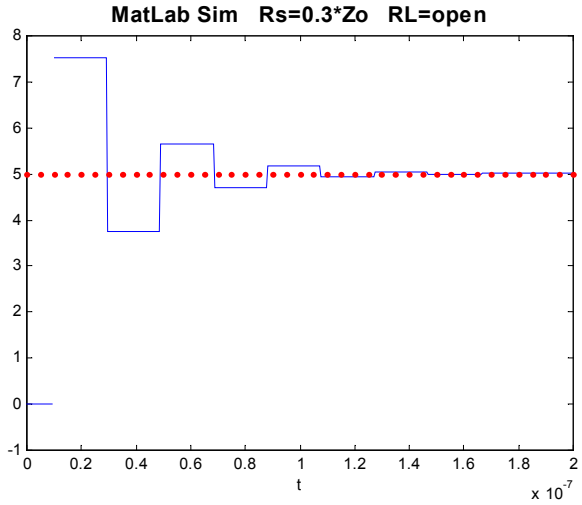
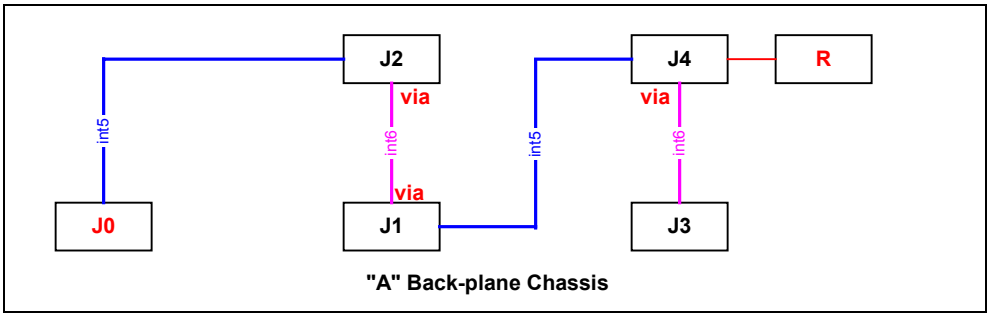
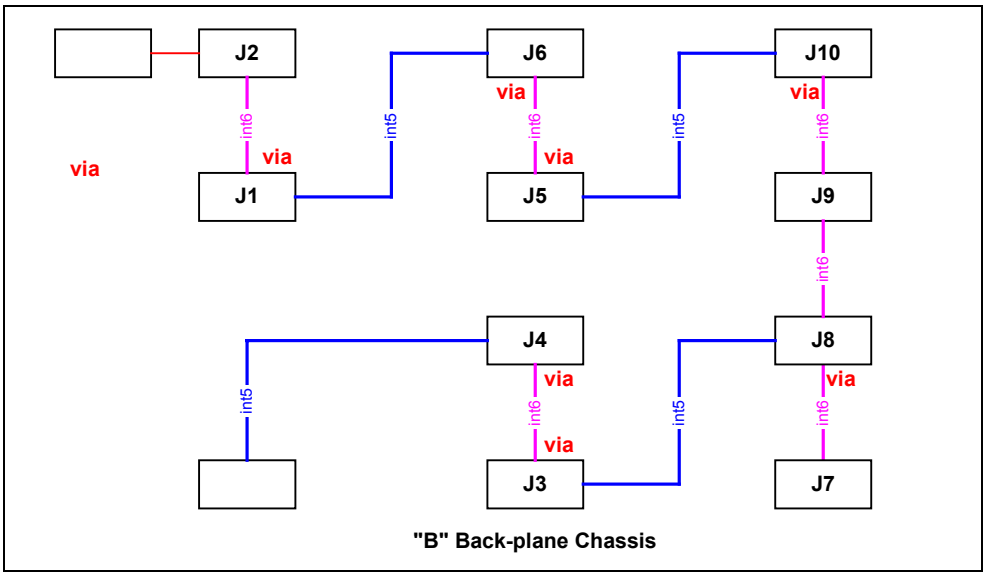


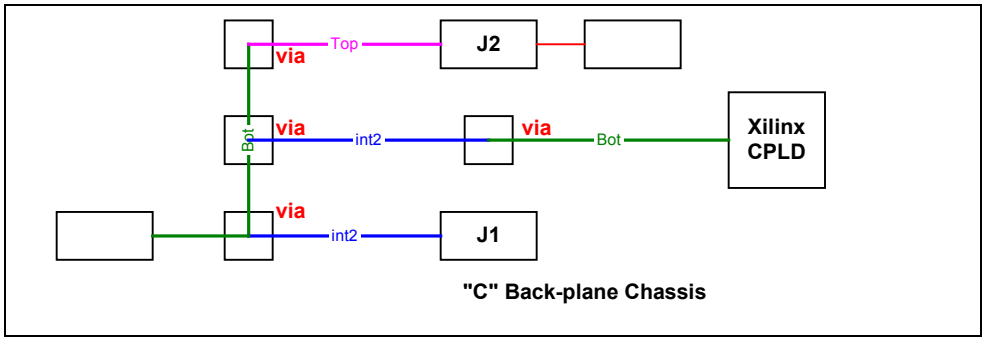
Fig.8 $R_S = 0.3Z_0 \quad R_L = \infty \,(open)$

Note that the clock signal is in good shape except lower amplitude in case of matched series termination and finite load impedance (Fig.5)

4. Verifications







The 3 figures above are clock traces on “A”, “B” and “C” back-planes. A **via** is a join of 2 traces at different layers. Reflection is not only caused by mismatched termination, but also by via!

So there should be **no via** for clock trace.

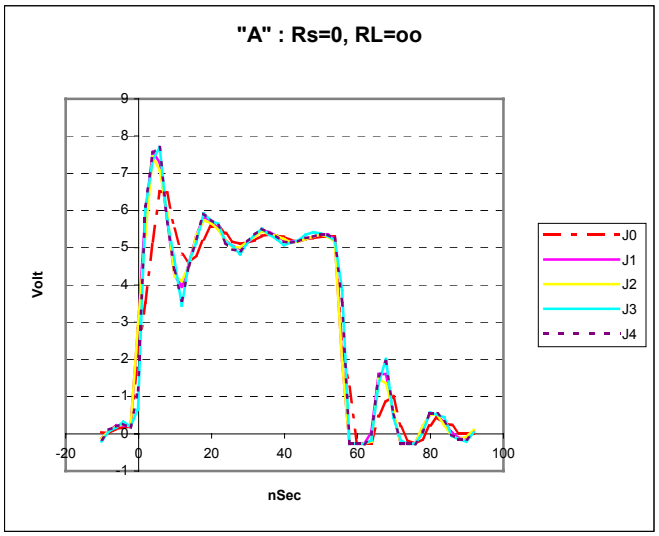
Below are waveforms 10 MHz captured using special low-capacitive LeCroy probe where 5V-amplitude clock is employed.

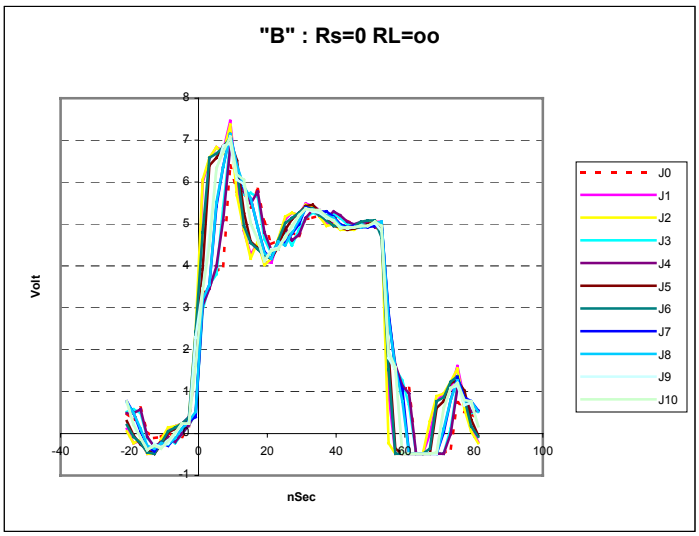
4.1. The Worst Case

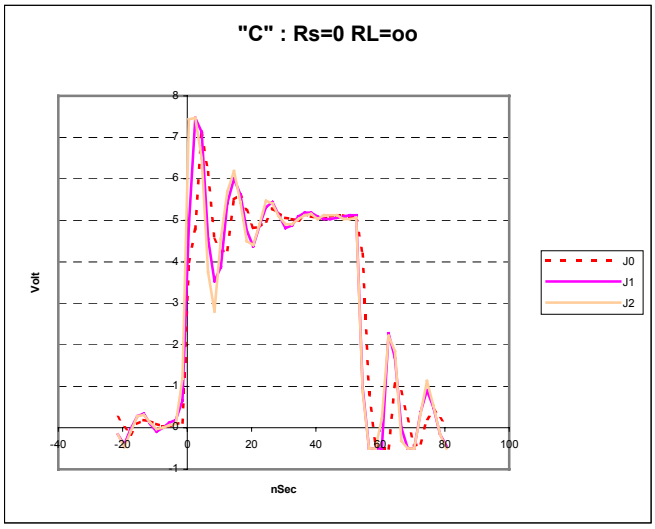
In simulation, we have a square-wave output for the step input in the worst case where Rs = 0, RL = open in Fig.4. In reality, we do not have zero output impedance for clock driver, so we expect the wave-form in Fig.8.

4.1.1. Rs = 0, RL = oo

Below are clocks signal taken from all connectors of "A", "B" and "C" back-planes.







4.1.2. Discussion

Because clock driver has non-zero output impedance, so all experimental results above are consistent with theoretical result in Fig.8. Note that clock signal has 5 V amplitude at connector as expected due to infinite load impedance.

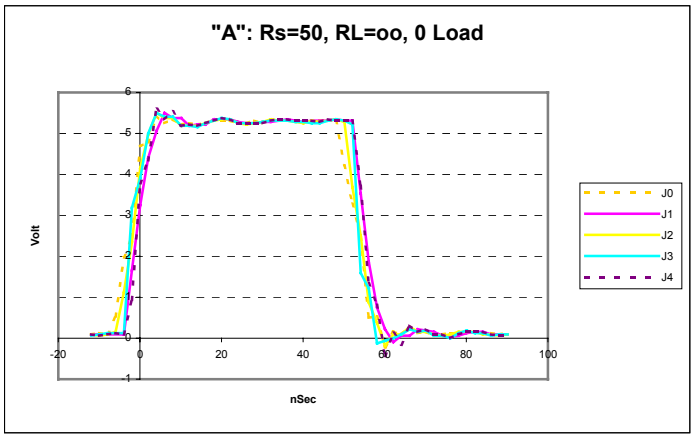
4.2. The Best Case

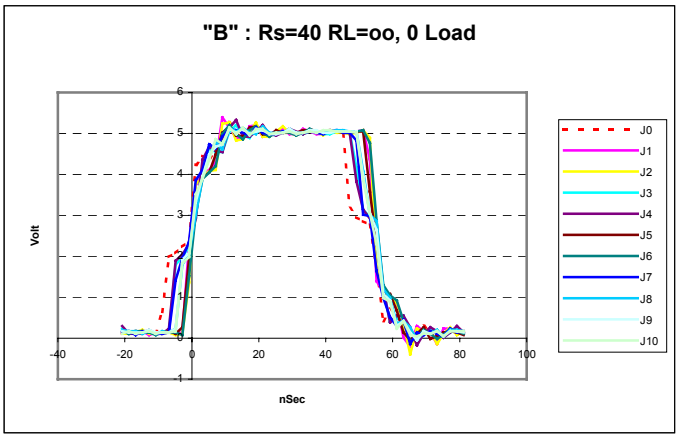
The best case is with series or parallel termination.

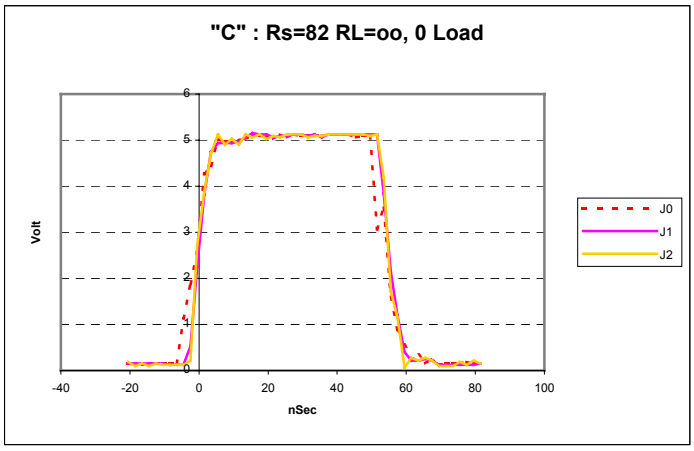
4.2.1. Series Termination

We need to consider 2 cases: with (finite load impedance) and without load (infinite load impedance)

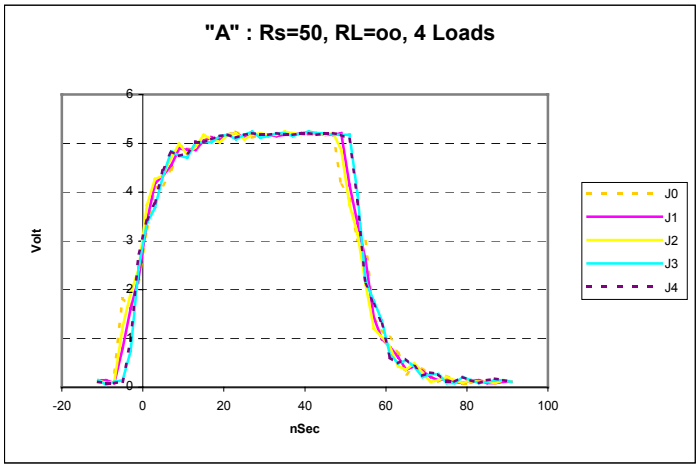
Without Load

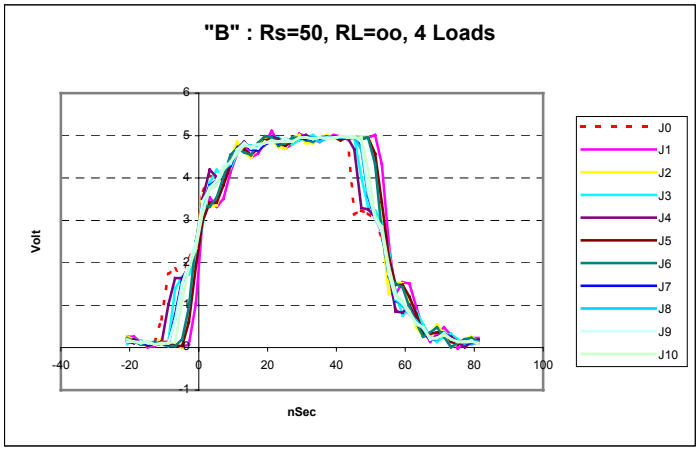


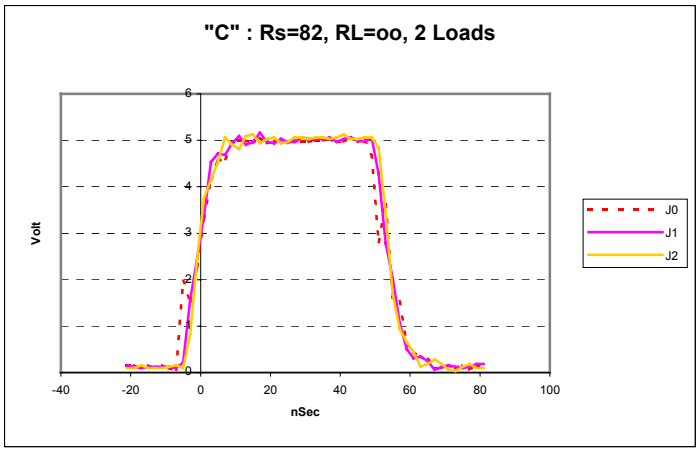




With Loads

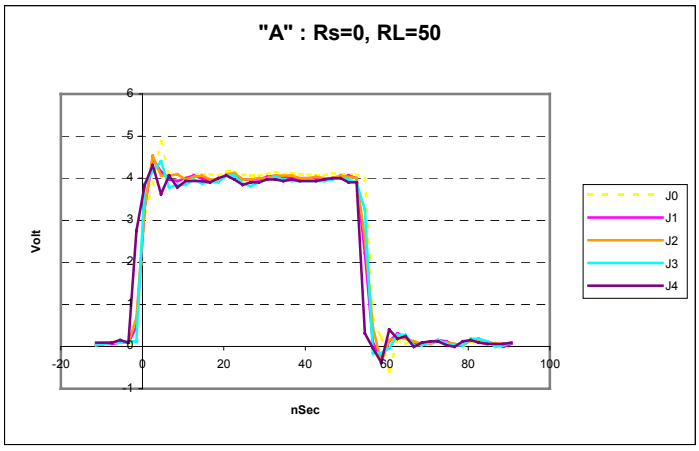


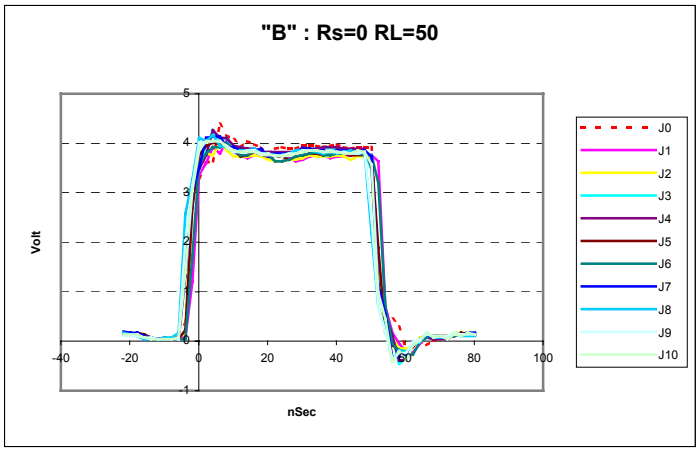


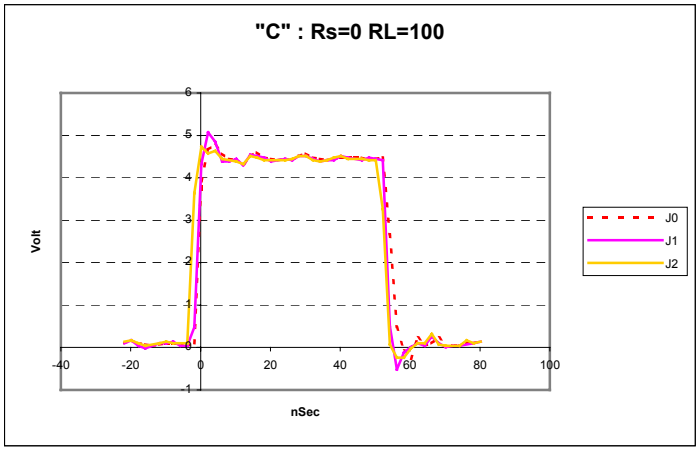


4.2.2. Parallel Termination

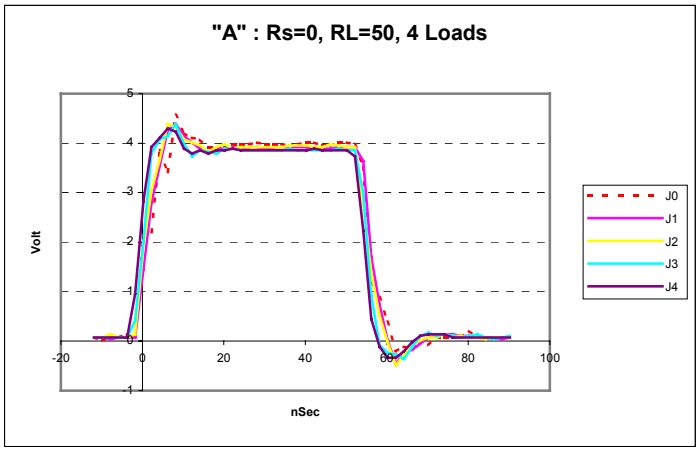
Without Load

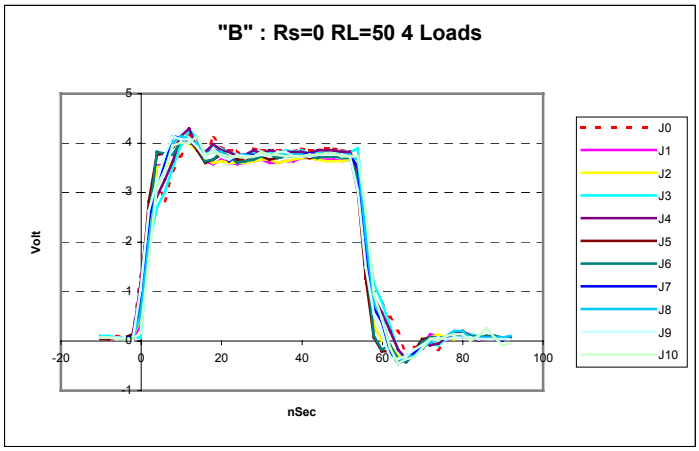


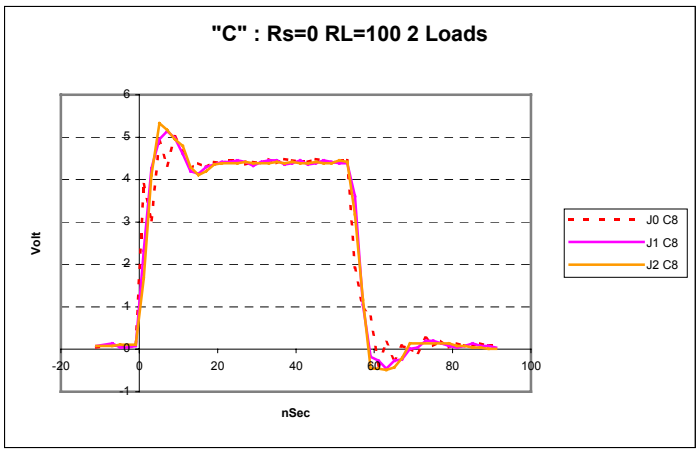




With Load







4.2.3. Discussion

There's no ringing for both matched series and parallel termination. We have 5V clock at load due to infinite impedance in series termination. However, the clock is less than 5 V in the parallel termination due to finite load impedance.

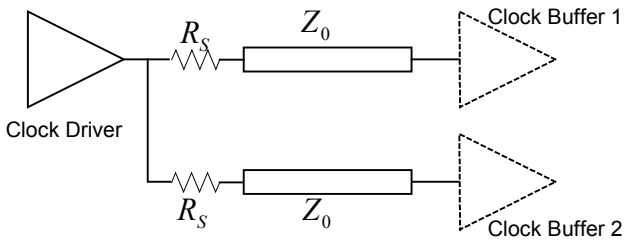
When there're some loads, clock is distorted due to vias, more number of vias, more distorted.

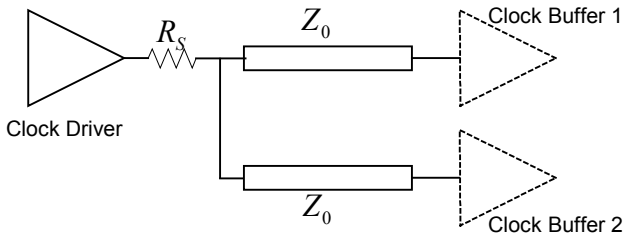
4.3. Single Clock with Multiple Traces

In principle, termination resistor is associated with its transmission line.

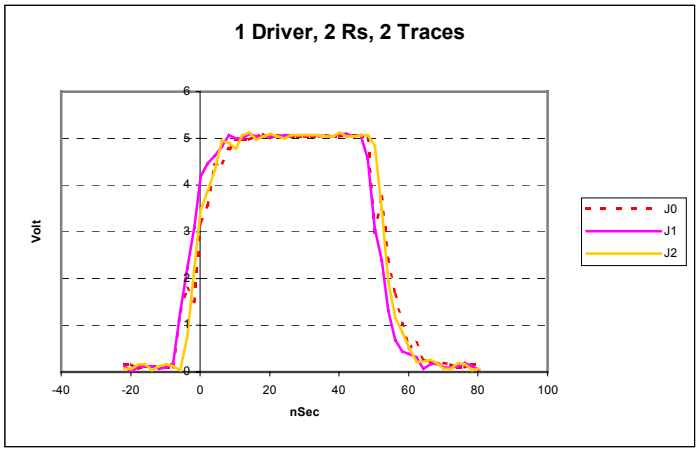
If we have a single clock source with 2 traces like of the same characteristic impedance, we have 3 cases below

1. If we use 2 drivers, 2 termination resistors and 2 traces; then it's very case of single clock, single trace discussed so far;
2. If we use 1 driver, 2 termination resistors and 2 traces, then it's also the case (1) above as seen below;
3. If we use 1 driver, 1 "*termination*" resistor and 2 traces, then it's a mismatched termination case as seen below;



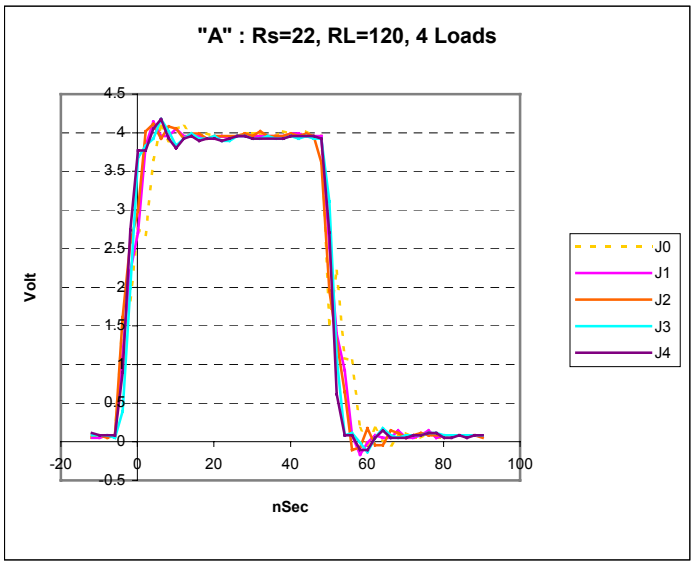


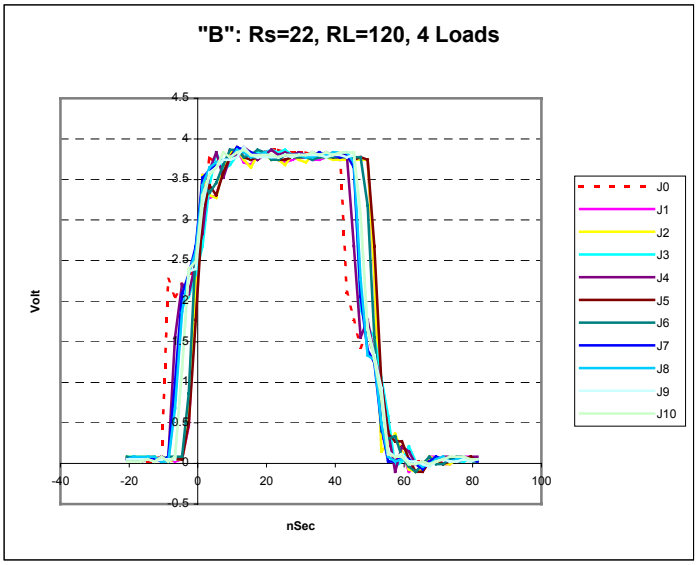
We'll use "C" back-plane to validate these issues as it has clock trace under impedance control, so both traces has roughly 100 Ohms.

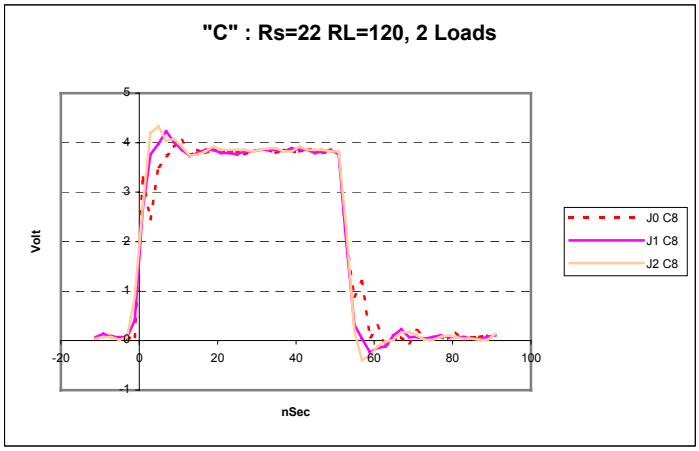


4.4. Study Cases

We'll use Rs = 22 Ohm and find RL for the best possible clock.







5. Conclusion

We have seen that improper termination causes reflections, and hence ringing . We may want to use some signal conditioning circuit to filter that ringing, but that technique may not be helpful in case of very high frequency.

To obtain clock of good quality

- there should be **no via** on clock trace, preferably on top or bottom of PCB;
- impedance control for clock trace;
- series resistor should be as close as possible to clock driver;
- parallel resistor should be at the end of clock trace;
- there should be both series Rs and parallel termination Rp resistors. So we can implement at will either (1) series termination : Rs = Zo, Rp=open or (2) Parallel Termination : Rs=0, Rp=Zo;
- each clock trace should have its own termination resistor.