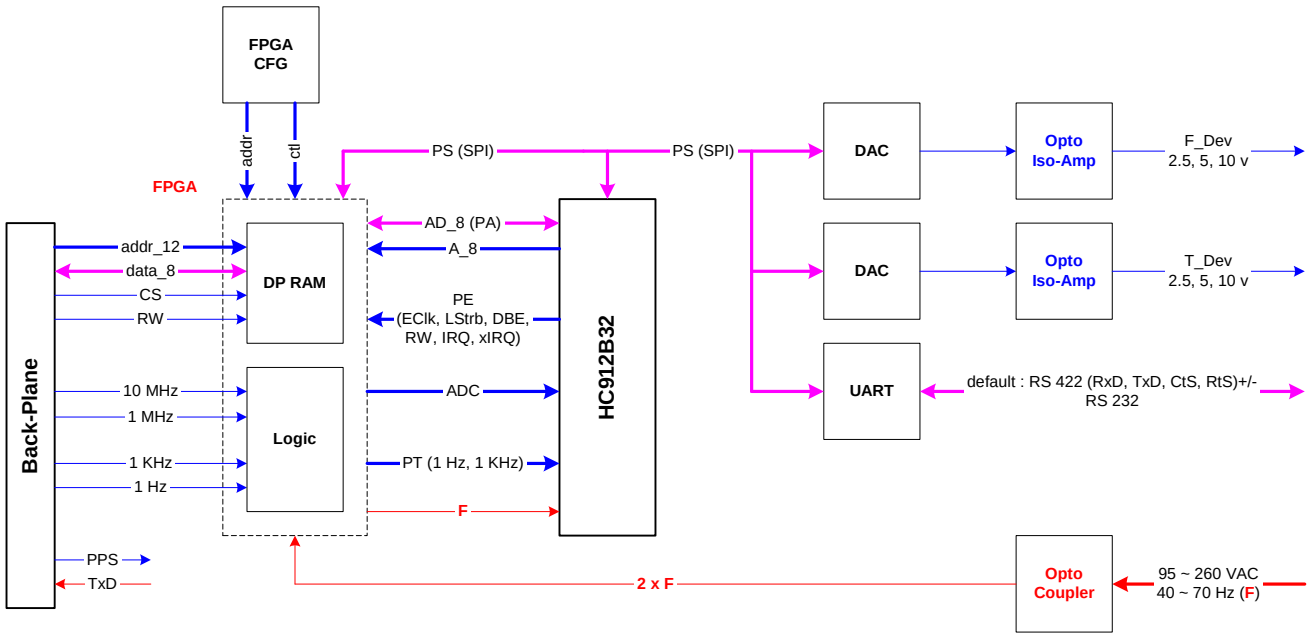
Notes on Design of
Frequency and Time Deviation Monitor

©Duy-Ky Nguyen 15 May 2003

1.1.1. Block Diagram



1) Parallel CFG FPGA
   - Mode M[2:0] = 3‘b110
   - CLLK : 16 MHz
   - CDAT : separate 8-bit data
   - CS = WS = 0
   - PRG, INIT (Reset), DONE
   - TDI_F (c); TD_F (TDO.c – TDI.f), TDO_F (f)

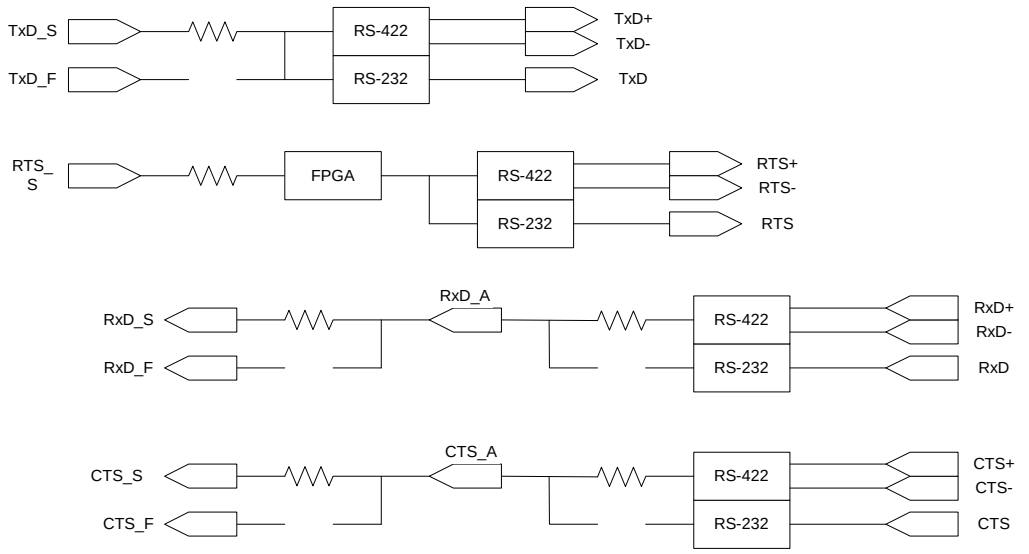
2) HC912B32 includes (i) 32 KB Flash for code, (ii) 728 B EEPROM for constant (baud, 50/60 Hz, …)
   - There are no PU/PD resistors for unused IO pins. They are input after reset. SW is expected to set them output for noise immunity.

3) SW selects either SPI or multiplexed AD to access DPRAM in FPGA.

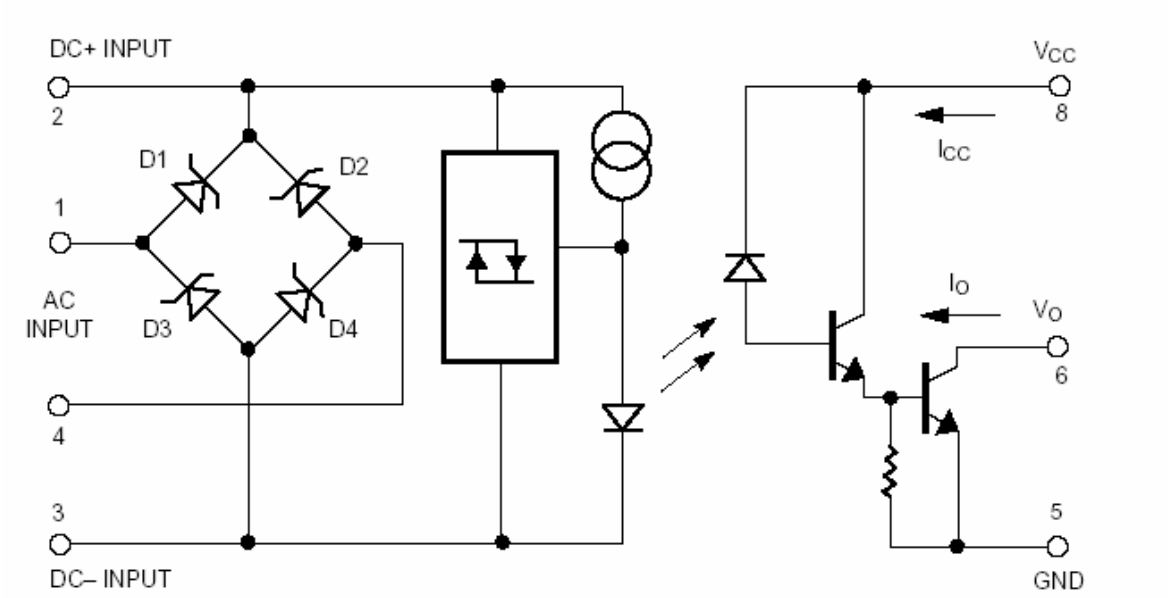
4) Unused pins of HC12 (PDLC) and FPGA are connected to header in case of connection using ribbon cable for testing purpose;

5) Serial Comm has HW hand-shake CTS RTS (default with MAX3100)

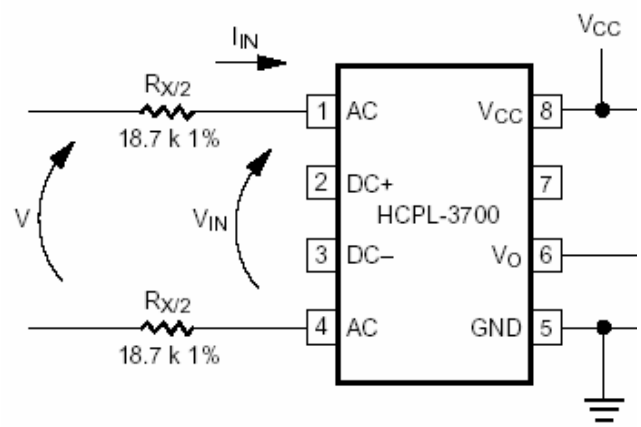
6) There are 3 ranges for T/F deviation outputs: 2.5, 5 and 10 v selectable using jumper.



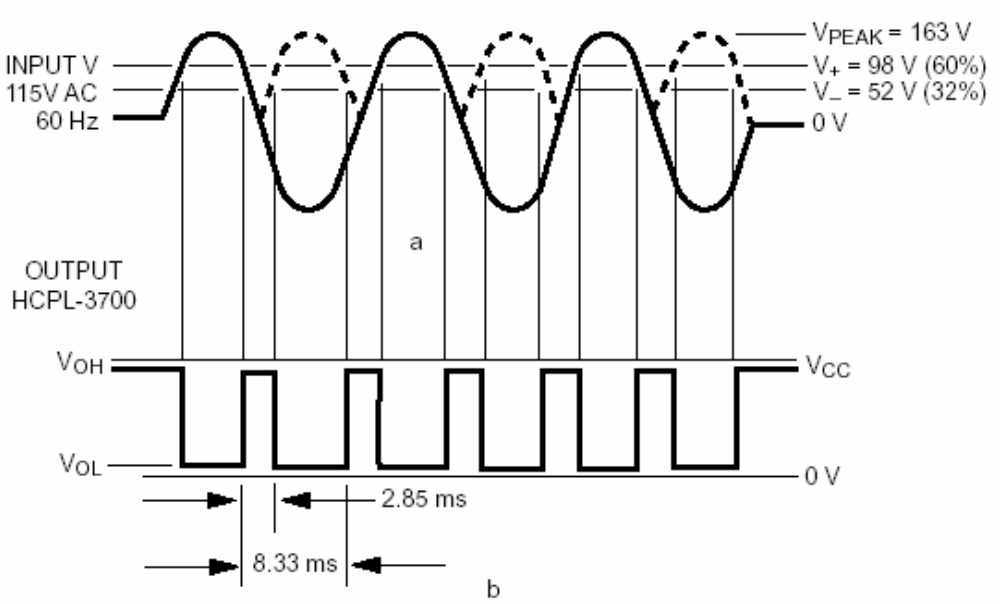
2. Power-Line Monitor



Block Diagram of the HCPL-3700 (Agilent Tech)



Interfacing an AC Voltage to an MPU using the HCPL-3700., V = 115 VAC, P_R = 116 mW (2.5 mA)



Output Waveforms of the HCPL-3700 Design in Figure 7 with no Filtering Applied, Vcc = 2 ~ 18 V

Design

Input 110 ~ 240 VAC, so the mode of Input Clamp Voltage is chosen with pins 2 & 3 open. Therefore we have following typical params

$$V_{IHC2} = |V_1 - V_4| = 6.7\ V$$
$$|I_{IN}| = 10\ mA$$
$$V_{peak} = 240 * 1.414 = 339.4\ V$$

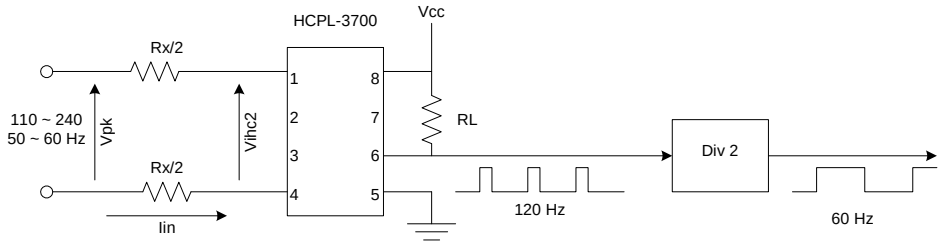
So

$$R_X = (V_{peak} - V_{IHC2}) / |I_{IN}| = 33.27\ KOhm$$

3. Opto-Coupler

3.1. AC Interface

Using HCPL-3700 from Agilent Technology.



For the mode of Input Clamp Voltage, we have

$$Vihc2 = 6.7\ v$$
$$|Iin| = 10\ mA$$

we have

$$Vr = Vpk - Vihc2 = 240*1.414 - 6.7 = 332.7\ v$$

So

$$Rx = Vr / |Iin| = 332.7 / 10 = 33.3\ K$$
$$R_{x/2} = 16.7\ K$$

Use $R_{x/2}$ = 18.7 K, 1%, so

$$P_{x/2} = (Vr/2)^2 / R_{x/2} = 1.5\ w$$

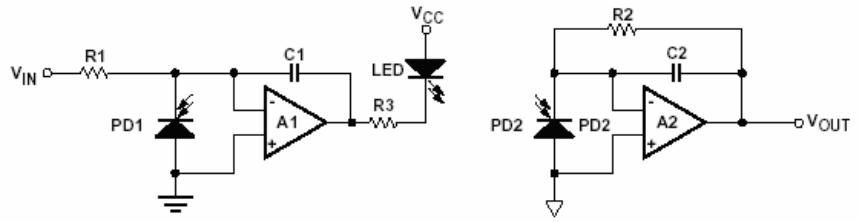
Choose

$R_{x/2}$ = 18.7 K, 1%, 1.5 w

Question:
Div2 is a flip-flop to divide 120 Hz for 60 Hz
RL is not required ???

3.2. Isolation Amplifier

Using HCNR-0201 from Agilent Technology.



Data sheet gives I_F = 1 ~ 20 mA, choose I_F = 2 mA, we have

$$R_3 = (V_{CC} - V_F)/I_F = 5/2 = 2.5\ K$$

Data sheet gives

$$I_{PD1} = K_1 * I_F = 0.5 * 2 = 1\ mA$$

so

$$R_1 = V_{IN} / I_{PD1} = 5/1 = 5\ K$$

as V_{IN} is an analog signal out of a 5-v DAC (Digital Analog Converter)

Data sheet gives

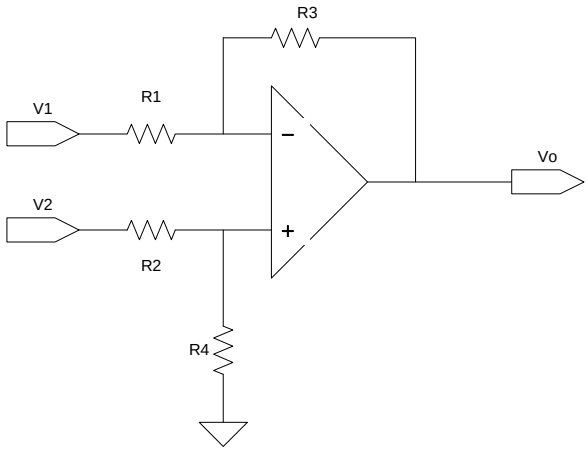
$$I_{PD2} = K_3 * I_{PD1} = 1 * 1 = 1\ mA$$

so

$$R_2 = V_{CC} / I_{PD2} = 5/1 = 5\ K$$

C_1 is for C_1R_1 to meet F_{max}
C_2 is for C_2R_2 to meet F_{max}

4. Op-Amp



Ideal Op-Amp has the following characteristics

$$V_- = V_+ \quad (1)$$

and

$$I_+ = I_- = 0 \quad (2)$$

Eqs (1) & (2) give

$$\frac{G_1V_1 + G_3V_0}{G_1 + G_3} = \frac{G_2V_2}{G_2 + G_4} \Rightarrow \frac{G_3V_0}{G_1 + G_3} = \left(\frac{G_2V_2}{G_2 + G_4} - \frac{G_1V_1}{G_1 + G_3}\right) \Rightarrow \frac{V_0}{1 + G_1/G_3} = \left(\frac{V_2}{1 + G_4/G_2} - \frac{V_1}{1 + G_3/G_1}\right)$$

or

$$V_0 = (1+G_1/G_3)\left(\frac{V_2}{1+G_4/G_2} - \frac{V_1}{1+G_3/G_1}\right) = (1+R_3/R_1)\left(\frac{V_2}{1+R_2/R_4} - \frac{V_1}{1+R_1/R_3}\right)$$

or

$$V_0 = -\frac{R_3}{R_1}V_1 + \left(1+\frac{R_3}{R_1}\right)\left(\frac{R_4}{R_2+R_4}\right)V_2 \qquad (3)$$

We want V_0 = -10 ~ +10 v, so we want 0 ~ -20 v for 1st term, and +10 v for 2nd. Therefore, for V_1 = 0 ~ 2.5 v we have

$$\frac{R_3}{R_1} = 8$$

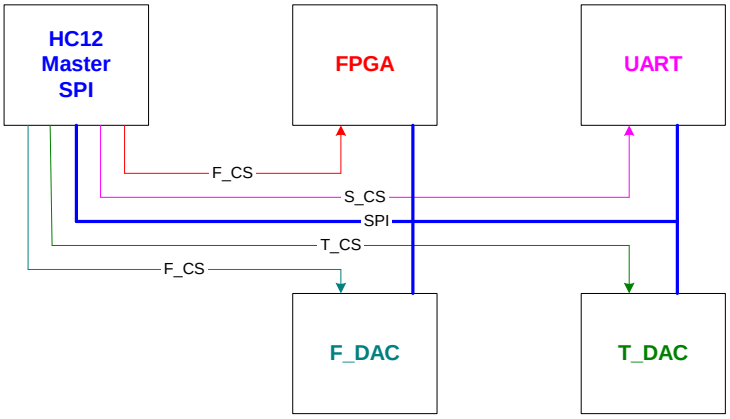
thus, for V_2 = 2.5 v, we have

$$(1+8)\frac{R_4}{R_2+R_4}2.5 = 10 \;\Rightarrow\; \frac{R_2}{R_4} = \frac{9*2.5}{10} - 1 = 1.25 = \frac{5}{4}$$

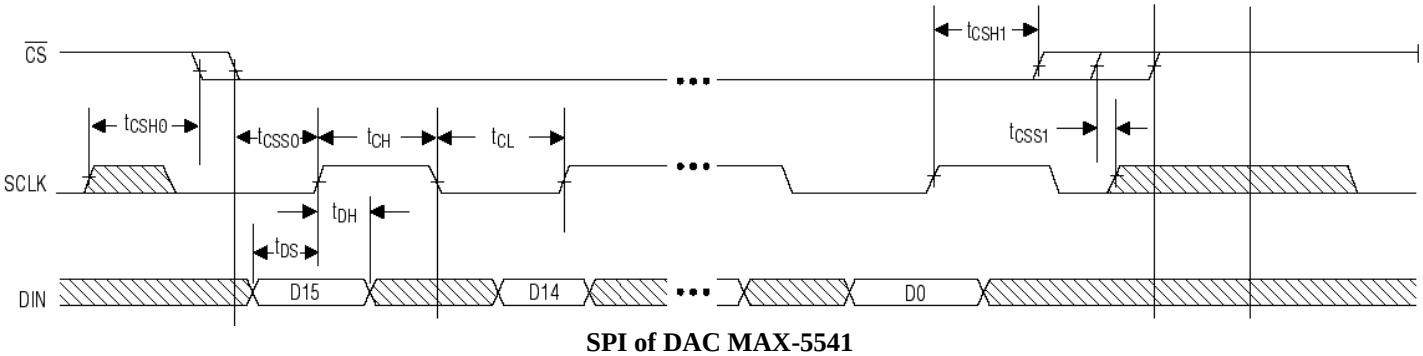
Note that these equations cannot be solved for non-inverting mode 0 ~ + 20 v.

5. SPI interface between HC12 abd FPGA

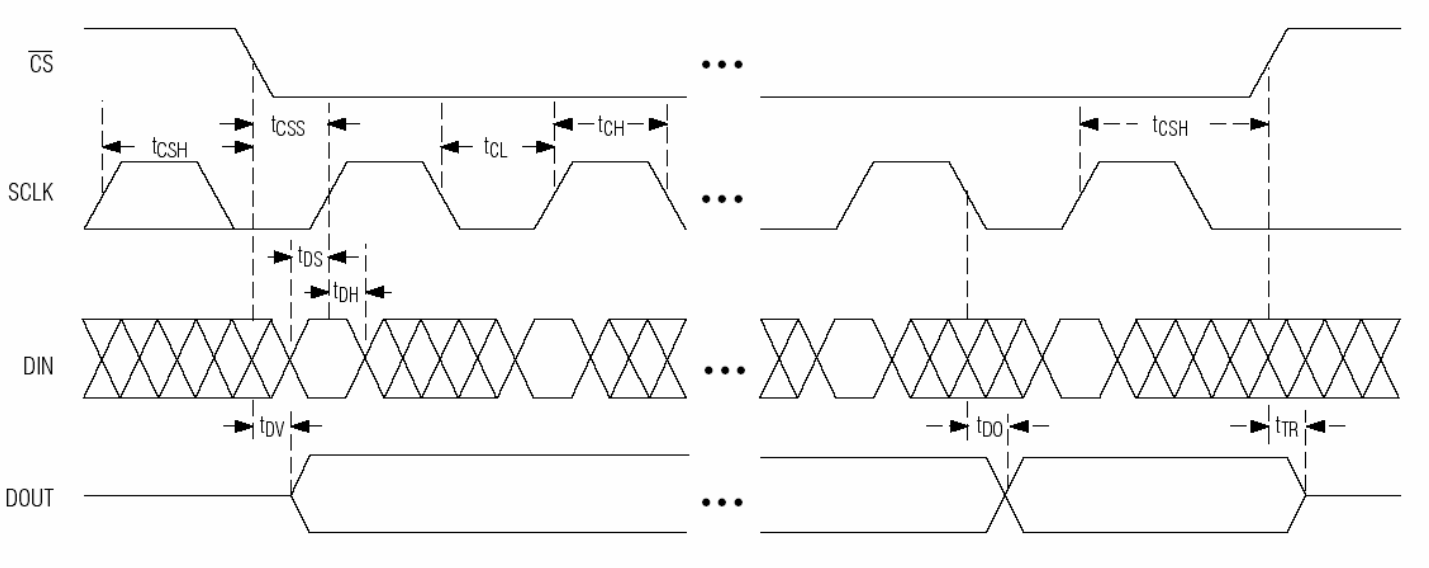
5.1. Requirements



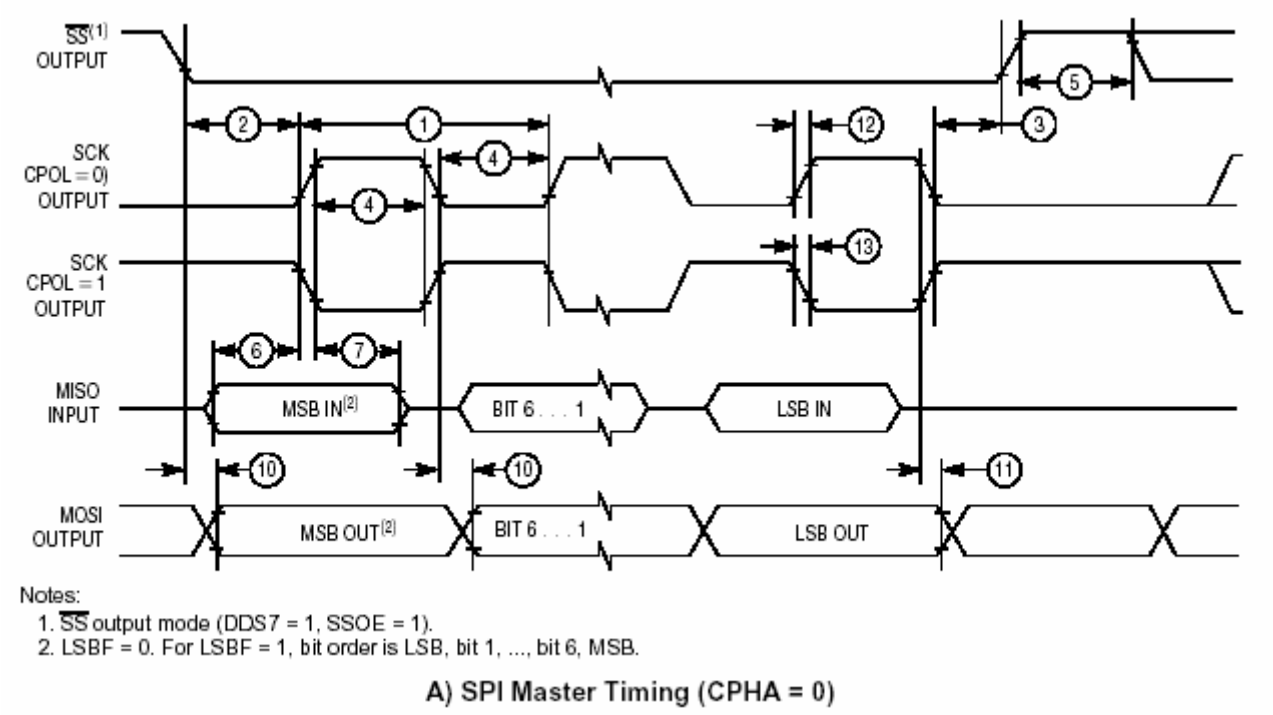
HC12 has master SPI interface with FPGA, DAC and UART. HC12 has 4 selectable SPI modes, but DAC and UART has only one that is CPOL=0, CPHA=0 in HC12. So FPGA will be implemented the same.



SPI of DAC MAX-5541

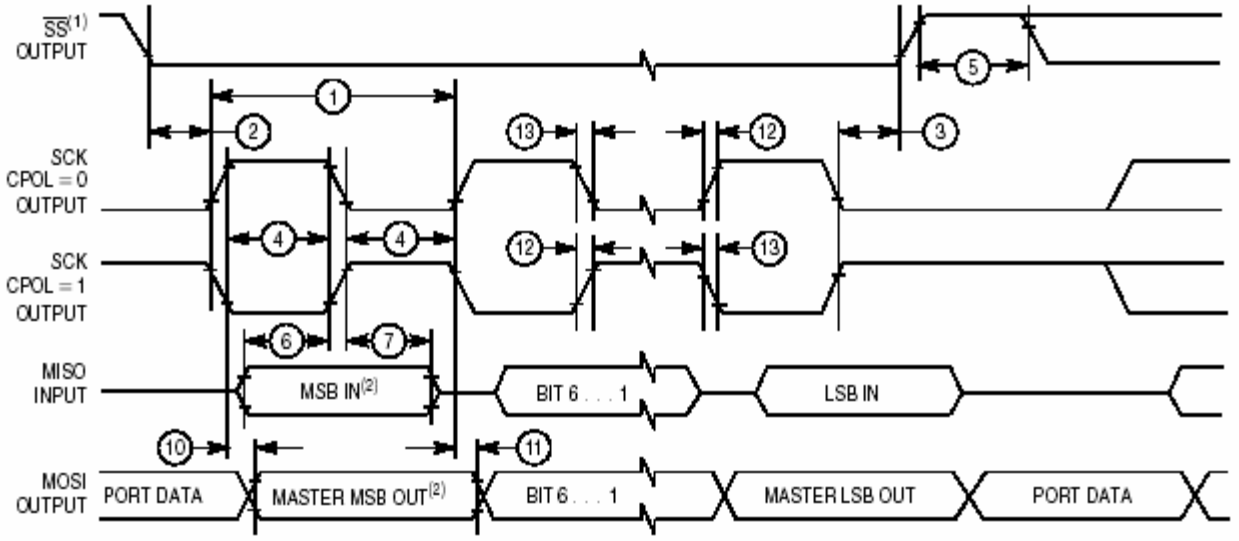


SPI of UART MAX-3100



Notes:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

A) SPI Master Timing (CPHA = 0)

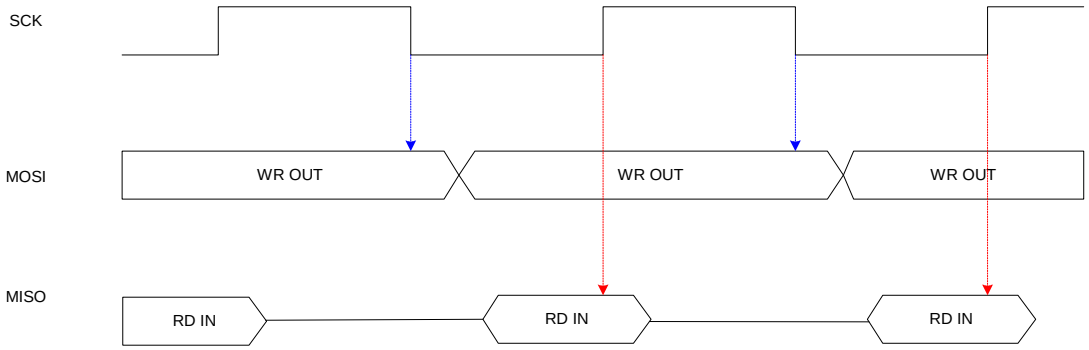


Notes:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

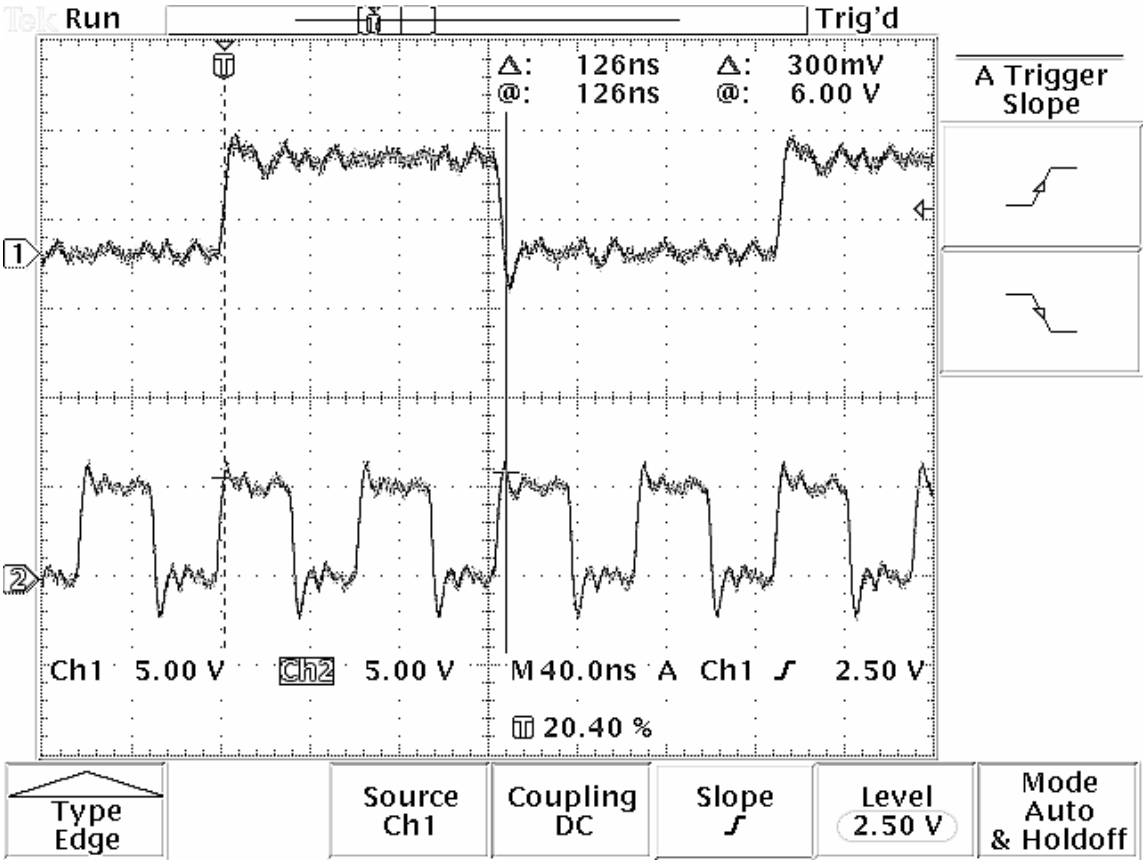
B) SPI Master Timing (CPHA = 1)

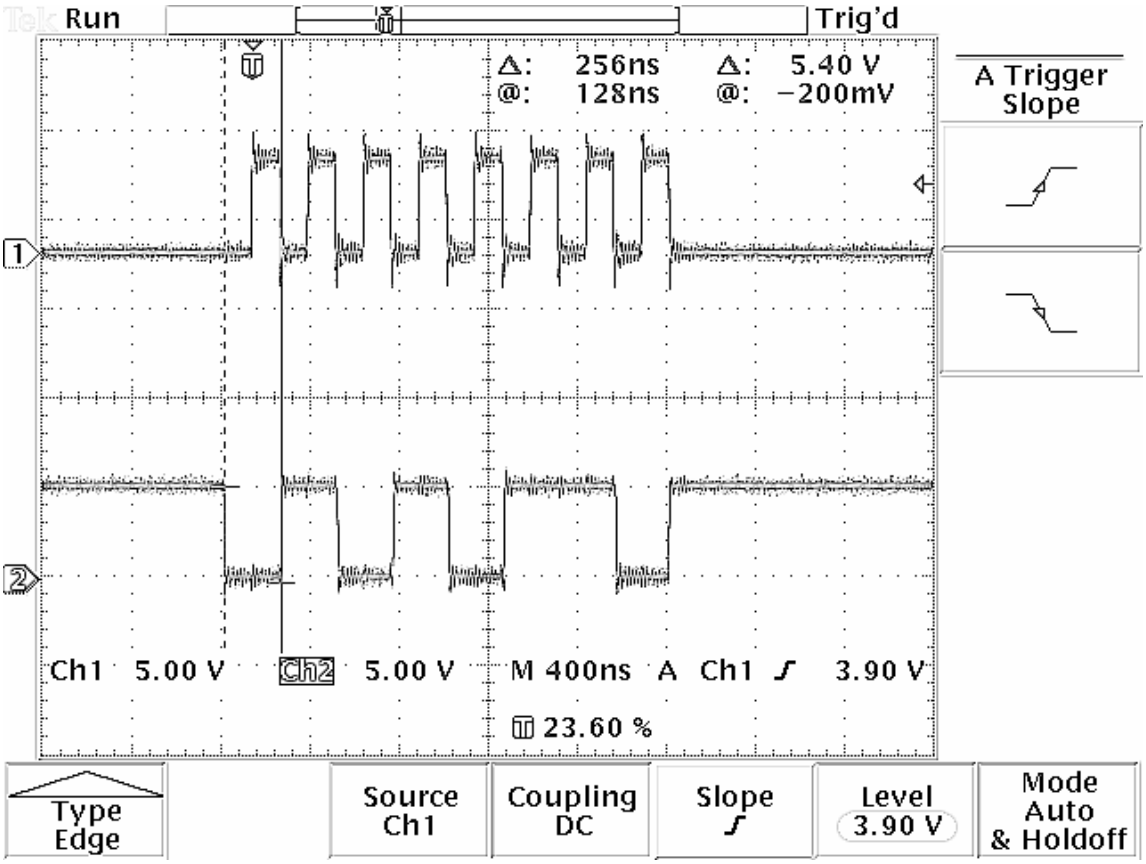
Num	Function(1)	Symbol	Min	Max	Unit
	Operating frequency	fOP	DC	1/ 2	E-clock frequency
1	SCK period	tSCK	2	256	tcyc
2	Enable lead time	tLead	1/ 2	—	tsck
3	Enable lag time	tLAG	1/ 2	—	tsck
4	Clock (SCK) high or low time	tWSCK	tcyc 30	128 tcyc	ns
5	Sequential transfer delay	tTD	1/ 2	—	tsck
6	Data setup time (inputs)	tSU	30	—	ns
7	Data hold time (inputs)	tHI	0	—	ns
8	Slave access time	tA	—	1	tcyc
9	Slave MISO disable time	tDIS	—	1	tcyc
10	Data valid (after SCK edge)	tV	—	50	ns
11	Data hold time (outputs)	tHO	0	—	ns
12	Rise Time Input Output	 tRI tRO	 — —	 tcyc 30 30	 ns ns
13	Fall Time Input Output	 tFI tFO	 — —	 tcyc 30 30	 ns ns

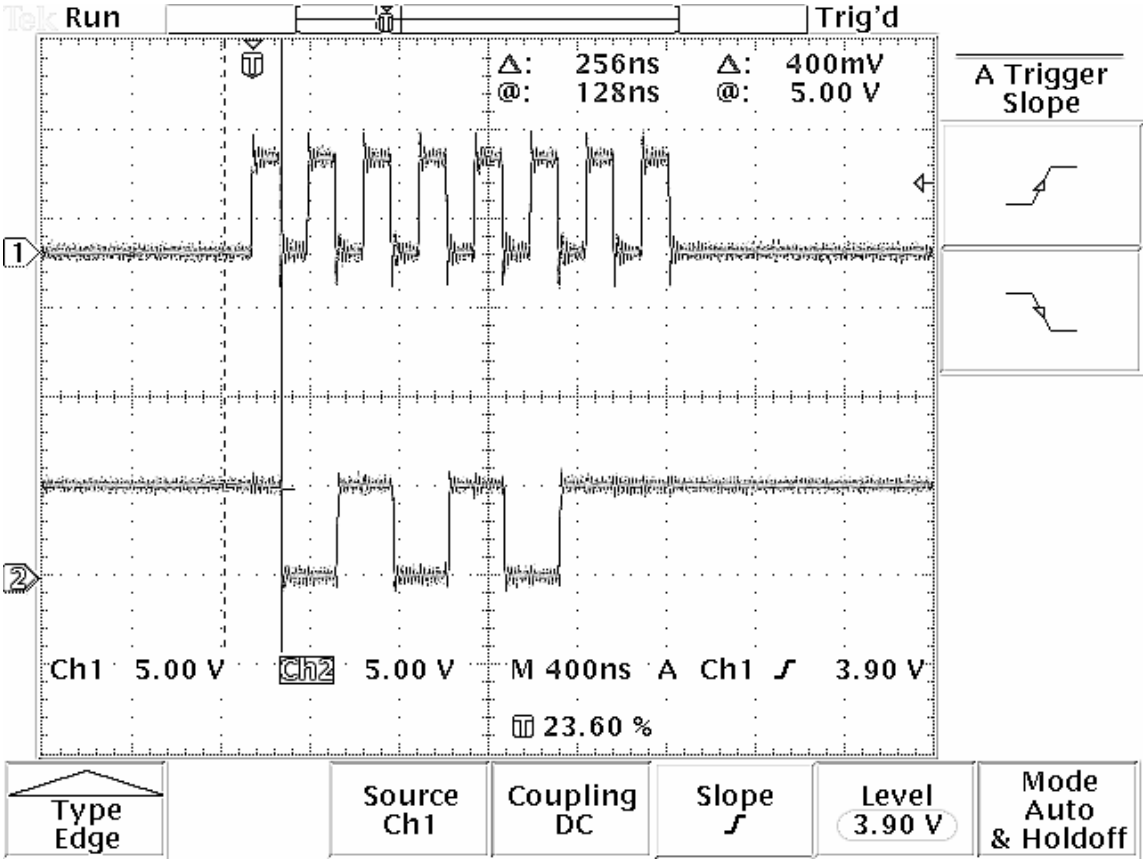
Below is expected SPI signals

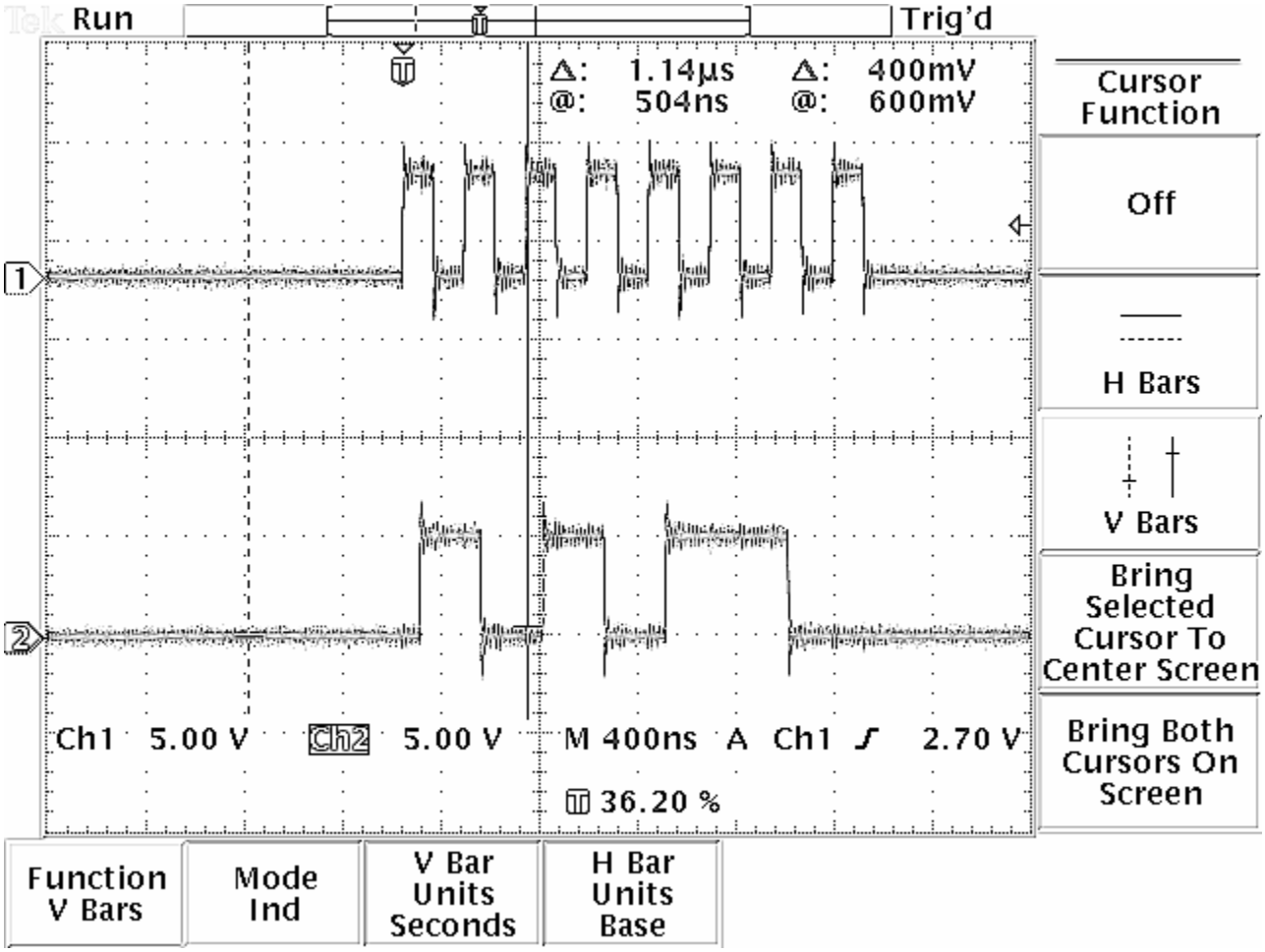


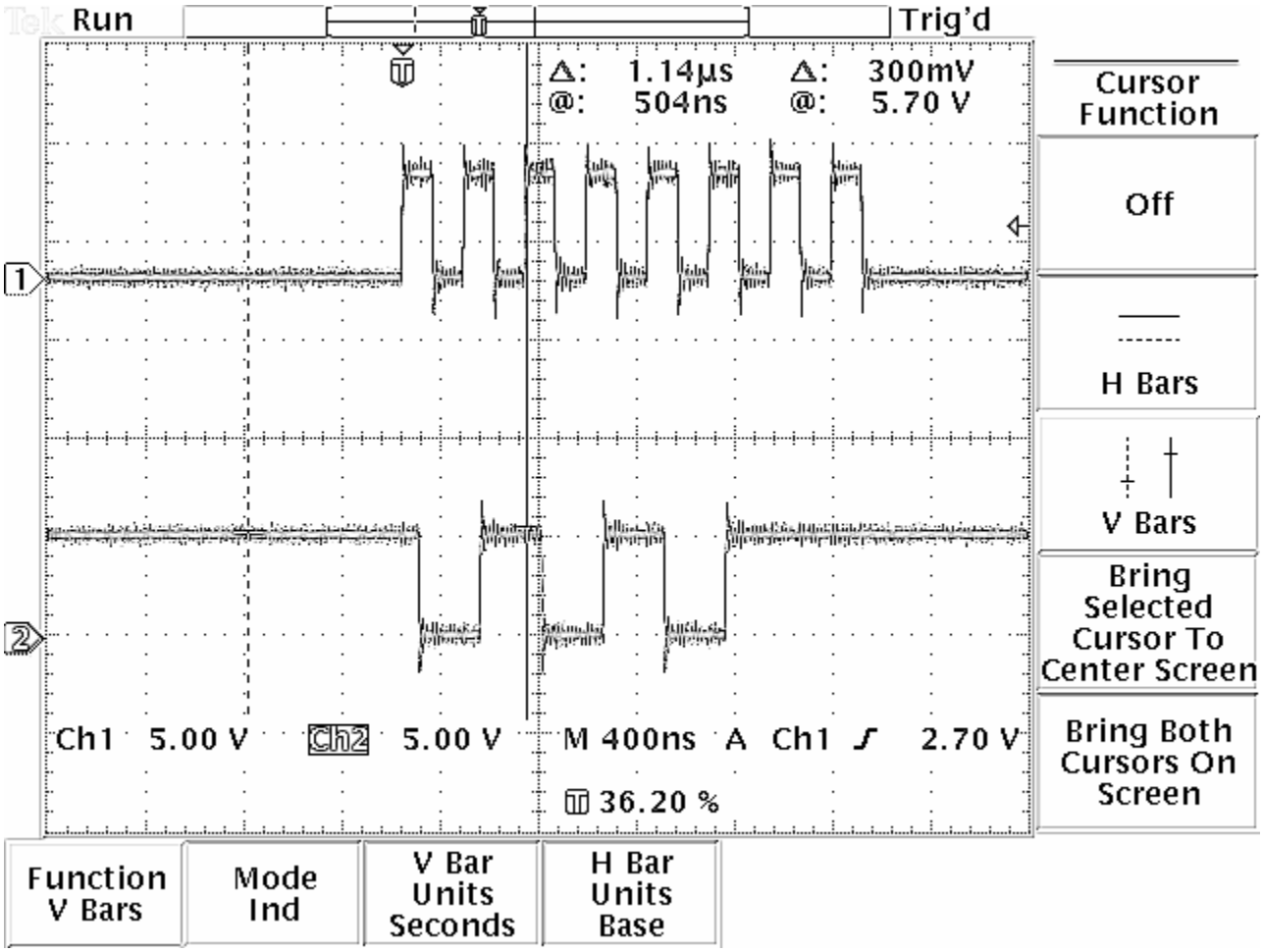
5.2. Implementation

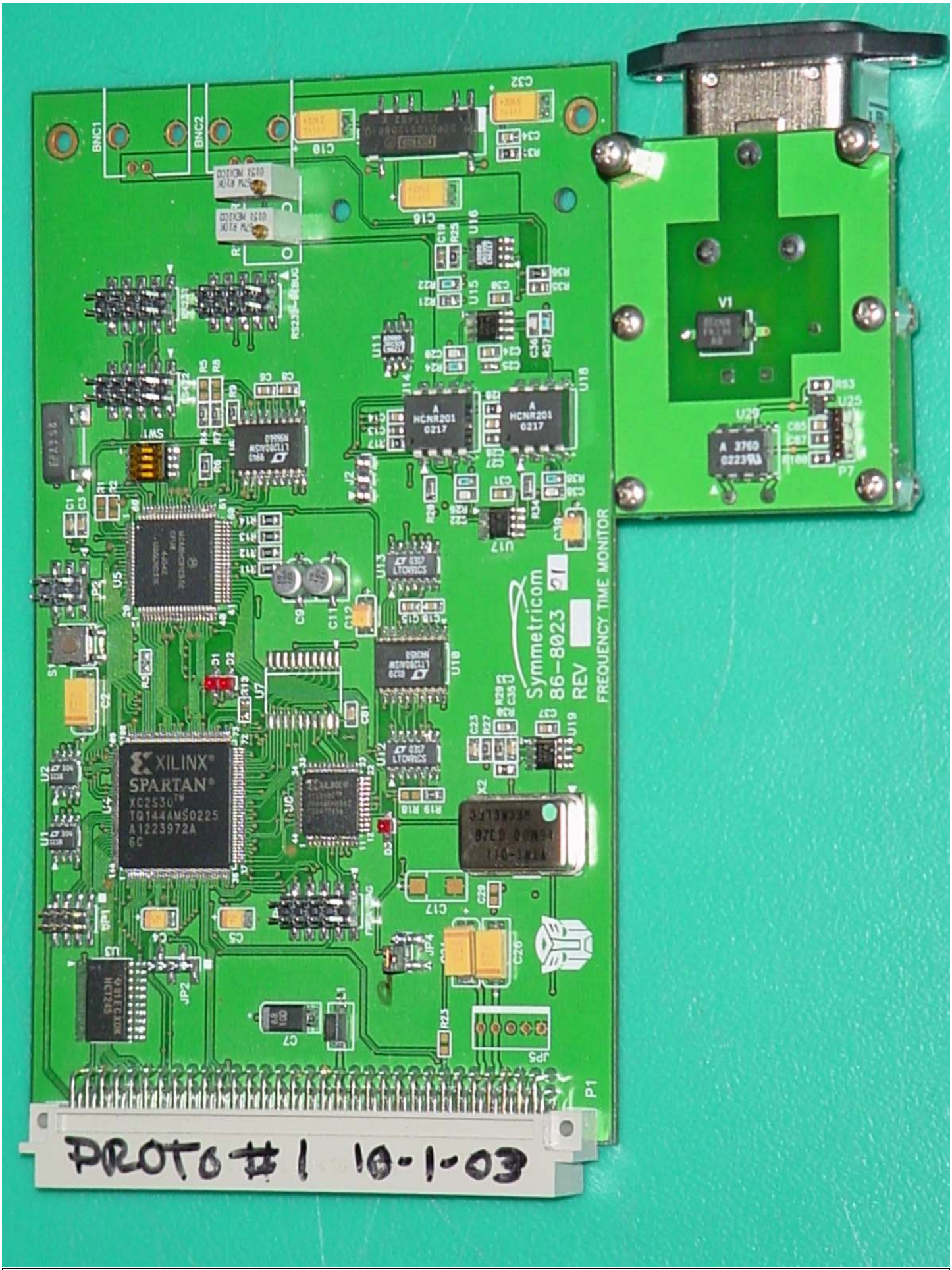





Run
Trig'd
Δ: 256ns Δ: 400mV
@: 128ns @: 5.00 V
A Trigger Slope
Ch1 5.00 V Ch2 5.00 V M 400ns A Ch1 3.90 V
23.60 %
Type Edge
Source Ch1
Coupling DC
Slope
Level 3.90 V
Mode Auto & Holdoff


Run
Trig'd
Δ: 1.14µs Δ: 400mV
@: 504ns @: 600mV
Cursor Function
Off
H Bars
V Bars
Bring Selected Cursor To Center Screen
Bring Both Cursors On Screen
Ch1 5.00 V Ch2 5.00 V M 400ns A Ch1 2.70 V
36.20 %
Function V Bars
Mode Ind
V Bar Units Seconds
H Bar Units Base


Run
Trig'd
Δ: 1.14µs Δ: 300mV
@: 504ns @: 5.70 V
Cursor Function
Off
H Bars
V Bars
Bring Selected Cursor To Center Screen
Bring Both Cursors On Screen
Ch1 5.00 V
Ch2 5.00 V
M 400ns A Ch1 2.70 V
36.20 %
Function V Bars
Mode Ind
V Bar Units Seconds
H Bar Units Base


BNC1
BNC2
V1
XILINX
SPARTAN
XC2S30
TQ144AMS0225
A1223972A
6C
Symmetricom
86-8023
REV
FREQUENCY TIME MONITOR
PROTO #1 10-1-03