Notes on Tahiti Design

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1.1.1. Introduction

1.2. Purpose

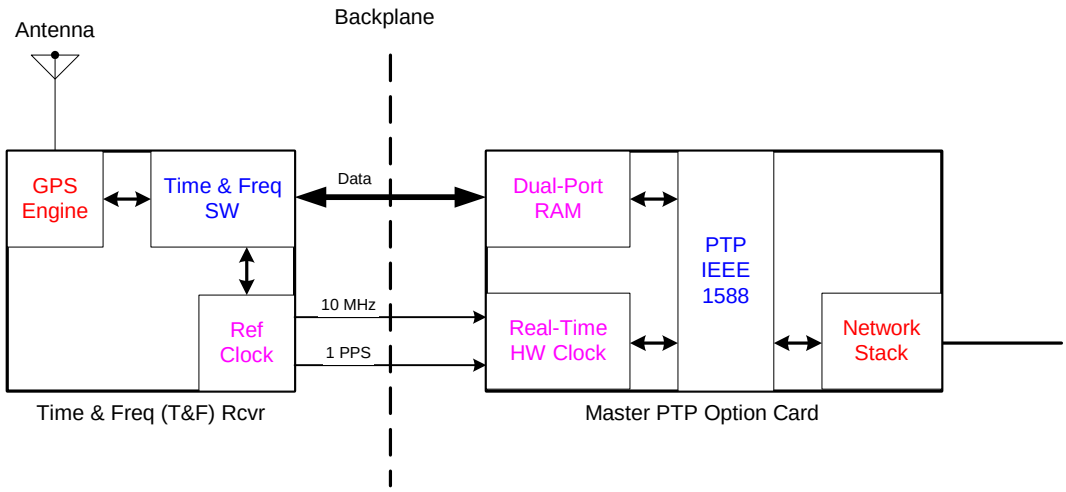
The purpose of this document is to capture the high level hardware design of an option card (A.K.A. “Tahiti”) for the Xli Time and Frequency Receiver in support of IEEE-1588-2002 Precise Time Protocol (PTP). The document covers hardware implementation concepts for both Master and Slave operation. This document is intended to guide the design approach and assist teams wishing to leverage Tahiti in future 1588 designs.

1.3. Reference Documents

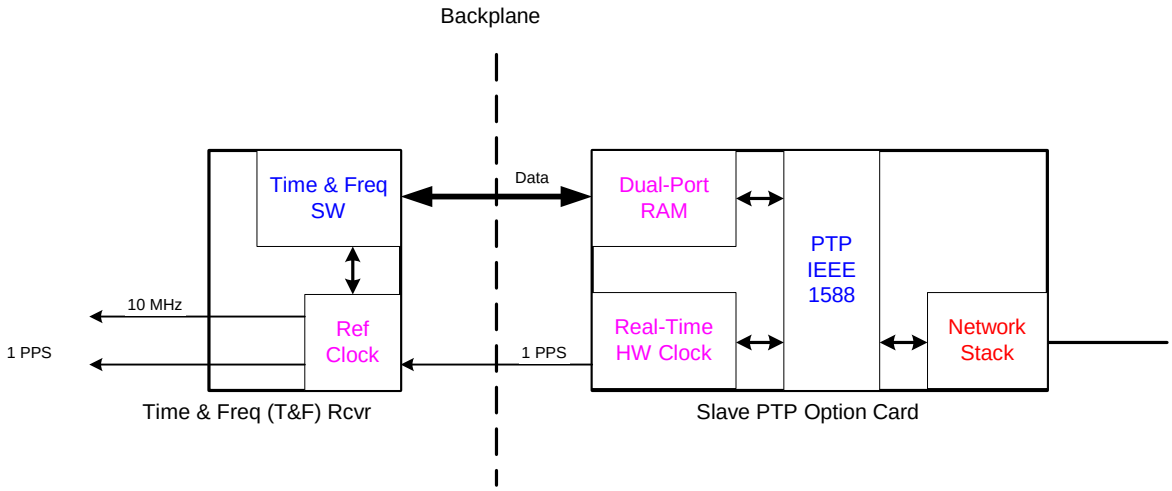
IEEE-1588-2002
Project Janus architecture, user interface, and specification
Project Quick Silver architecture
Project Maui architecture and design
IEEE 1588 Hardware Requirements
Xli/GPS Software Architecture
www.ietf.org archive of all RFC’s

2. High Level System Design

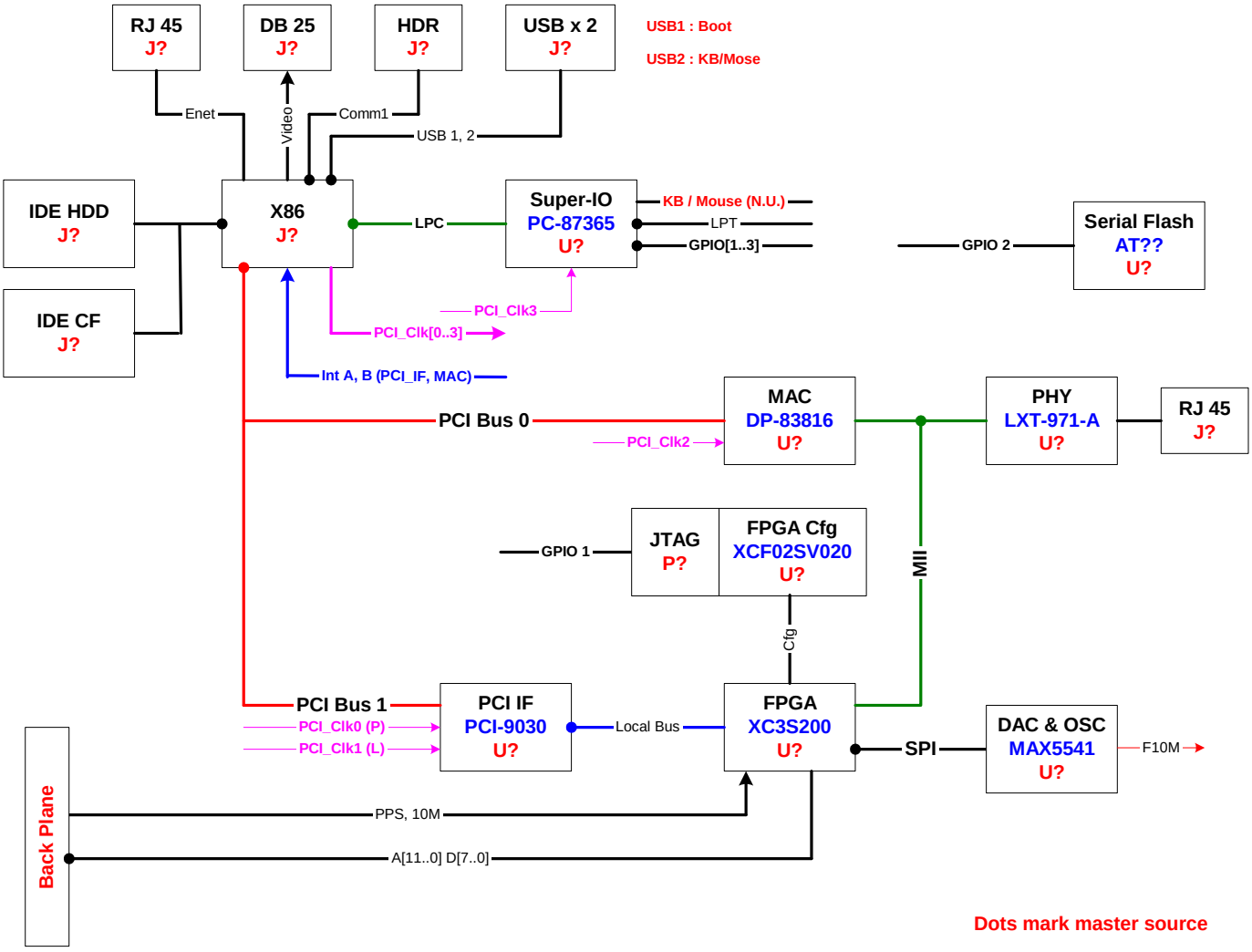
Sample Master Configuration



Sample Slave Configuration



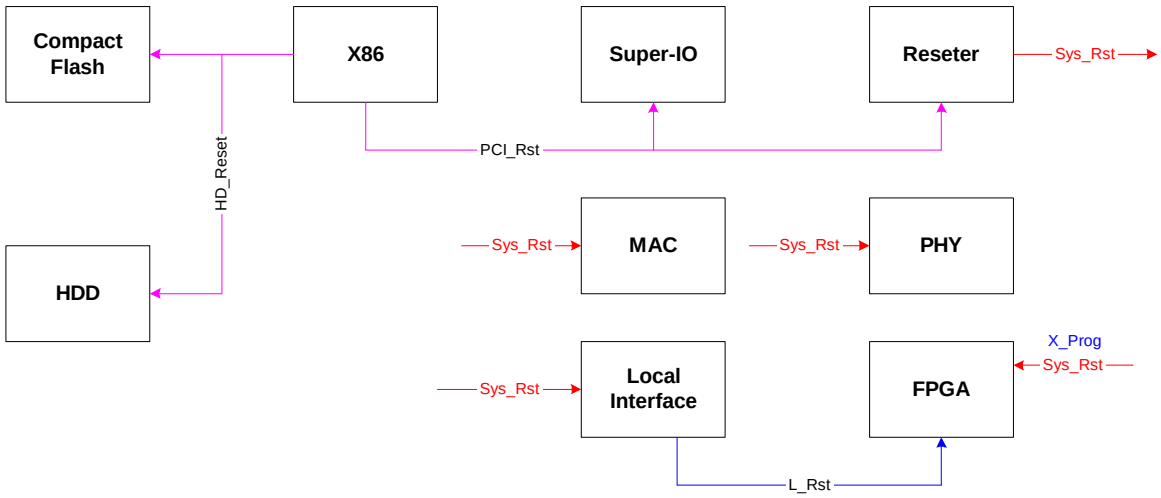
3. Hardware Interconnection Diagrams



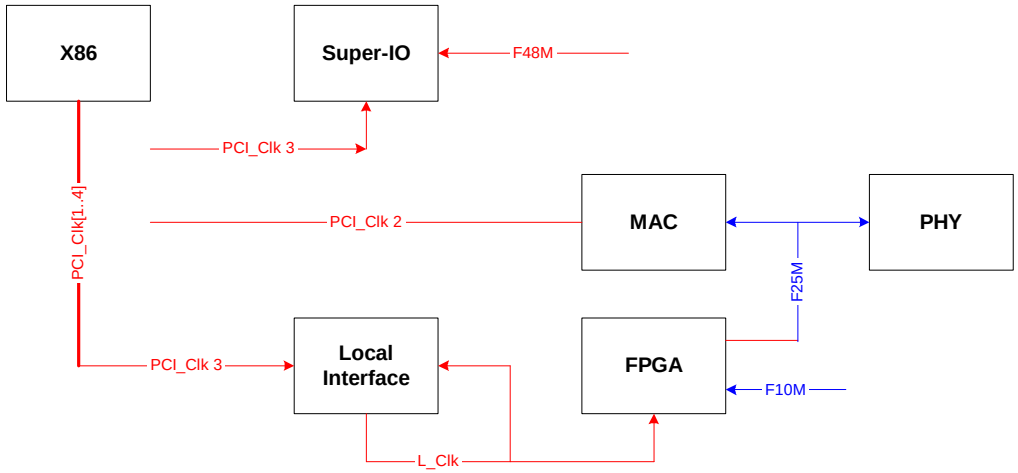
- Serial Flash for non-volatile X86 data;
- FPGA configured either by FPGA Cfg PROM or by X86 whose flash holds FPGA image;

All detailed of connections between modules are to follow.

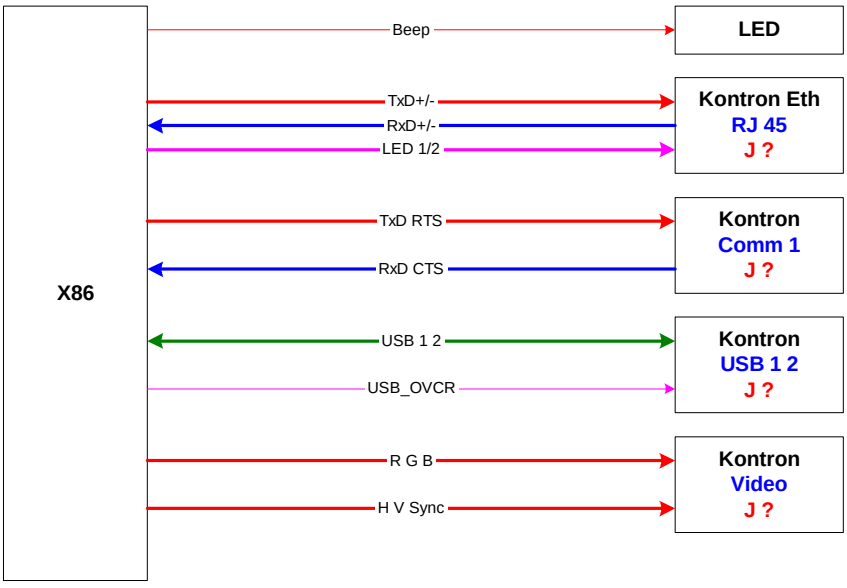
3.1. Reset



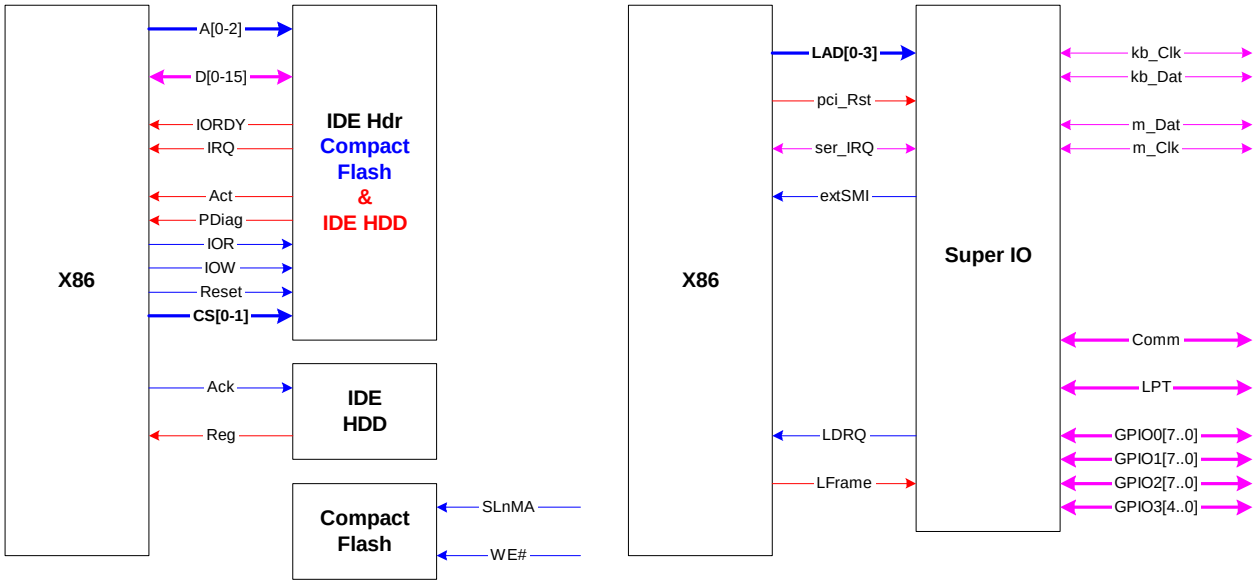
3.2. Clock

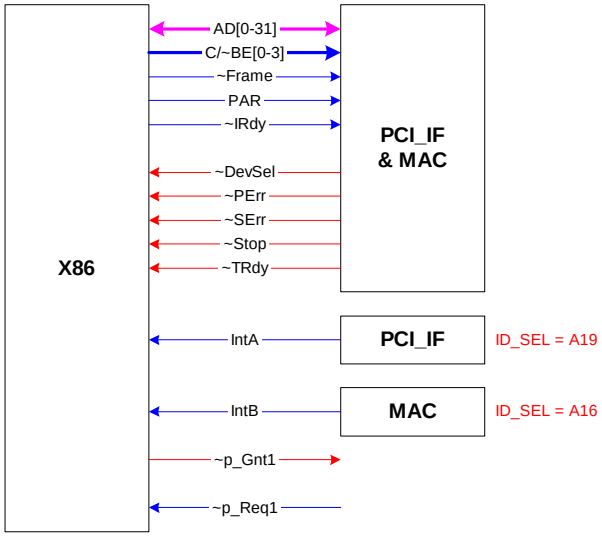


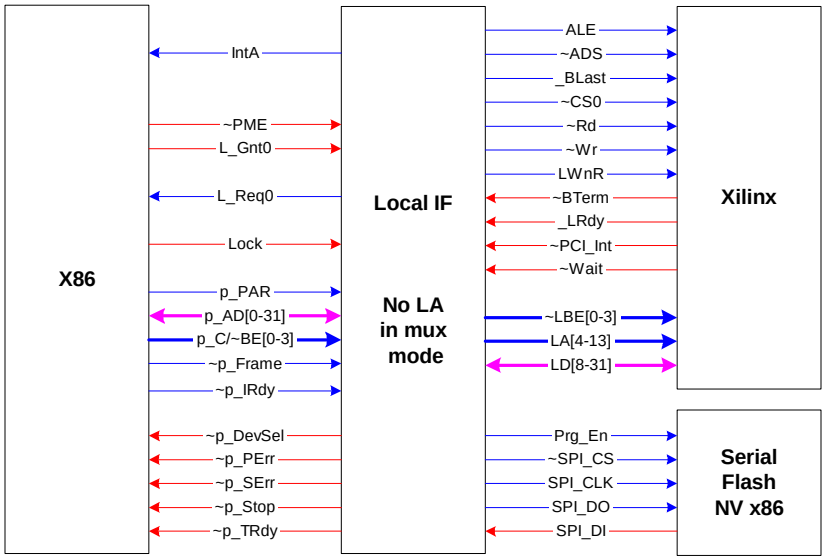
3.3. Comm Bus

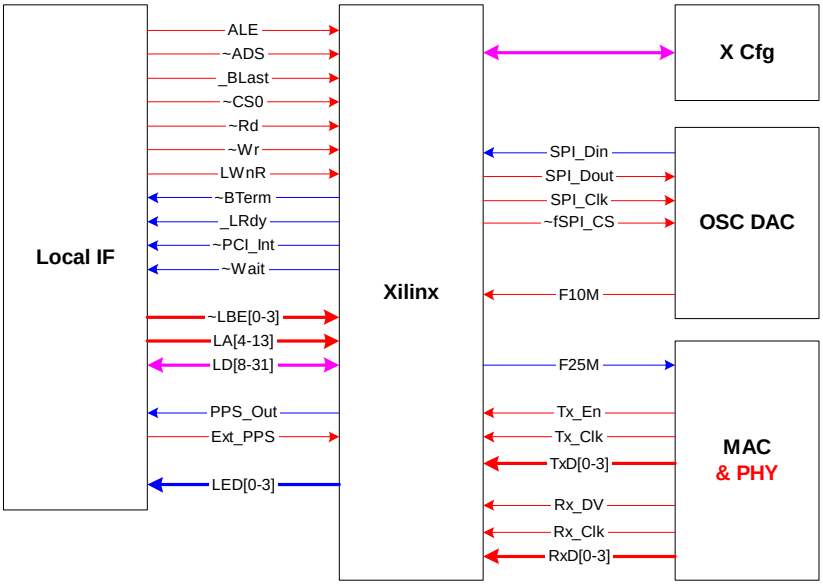


3.4. Data Bus


X86
A[0-2]
D[0-15]
IORDY
IRQ
Act
PDiag
IOR
IOW
Reset
CS[0-1]
IDE Hdr
Compact
Flash
&
IDE HDD
Ack
Reg
IDE
HDD
SLnMA
WE#
Compact
Flash
X86
LAD[0-3]
pci_Rst
ser_IRQ
extSMI
LDRQ
LFrame
Super IO
kb_Clk
kb_Dat
m_Dat
m_Clk
Comm
LPT
GPIO0[7..0]
GPIO1[7..0]
GPIO2[7..0]
GPIO3[4..0]


X86
AD[0-31]
C/~BE[0-3]
~Frame
PAR
~IRdy
~DevSel
~PErr
~SErr
~Stop
~TRdy
PCI_IF
& MAC
IntA
PCI_IF
ID_SEL = A19
IntB
MAC
ID_SEL = A16
~p_Gnt1
~p_Req1



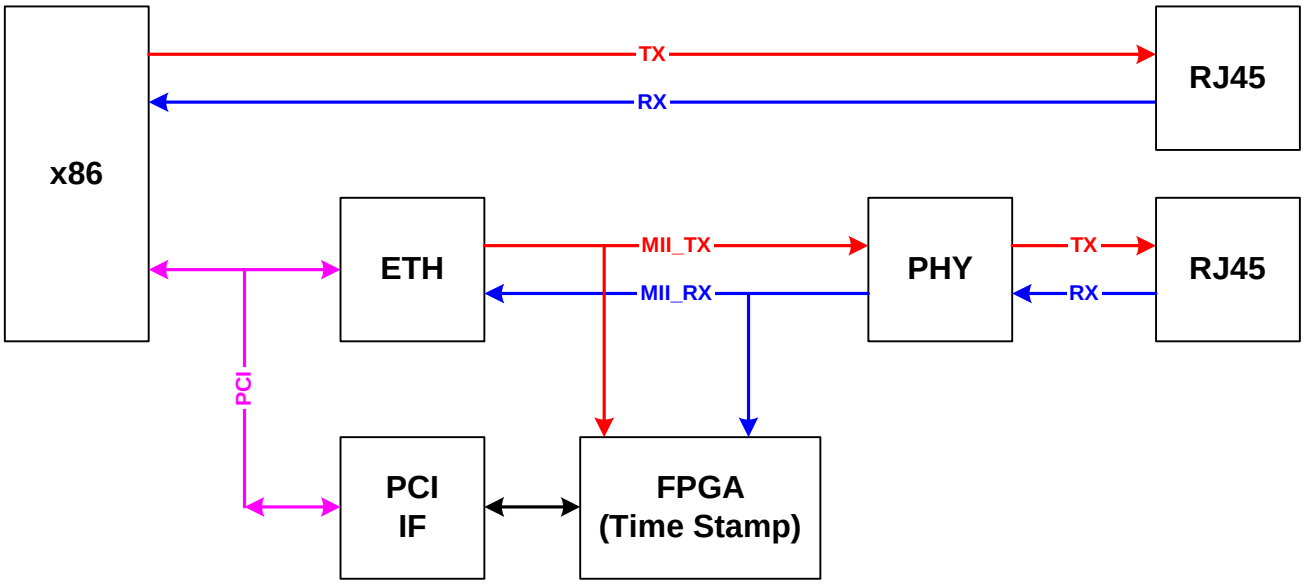


FPGA could be configured either by a special FPGA configuring flash or by HC12 with the image stored in HC12 internal flash.

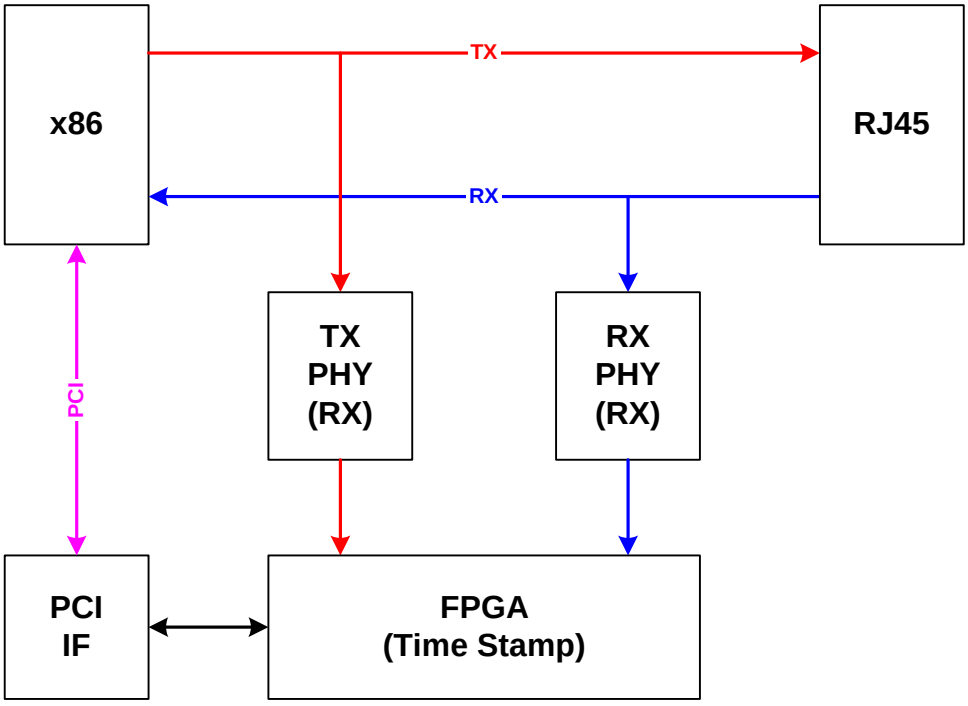
4. PTP IEEE-1588 Time Stamp Archtiecture

The PTP provides more precise time sync as it counts delay time between master and slave clocks. Basically, it has 2 types of message. The first one SYNC message is used for offset time. The 2nd one DELAY_REQ is for delay time where it does assume *symmetrical topology*, hence the delay time is half of round-trip delay. This is a very important requirement of PTP foundation.

Xli-QuickSilver architecture (arch_1)

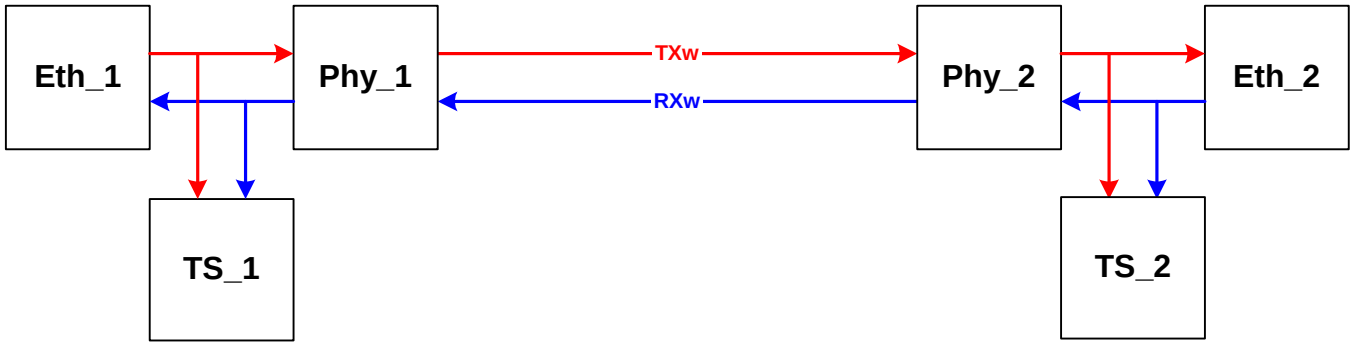


Zurich University architecture (arch_2)



To check their symmetrical topology, we need to look at both master and slave clocks.

For arch_1, we have



For one way, we have

$$t_{TX} = t_{TXp1} + t_{TXw} + t_{RXp2} \tag{1}$$

and the other way has

$$t_{RX} = t_{TXp2} + t_{RXw} + t_{RXp1} \tag{2}$$

where copper trace propagation delays are in order of pico-second and ignored.

It's safe to assume the same wire delay in both directions, ie

$$t_{TXw} = t_{RXw} \tag{3}$$

But, it's possible to have different delay in both directions within the PHY chip as they have different logic jobs to deal with. One converts digital code to line code and the other does the reverse job, so

$$t_{TXp1} \neq t_{RXp1} \quad and \quad t_{TXp2} \neq t_{RXp2} \tag{4}$$

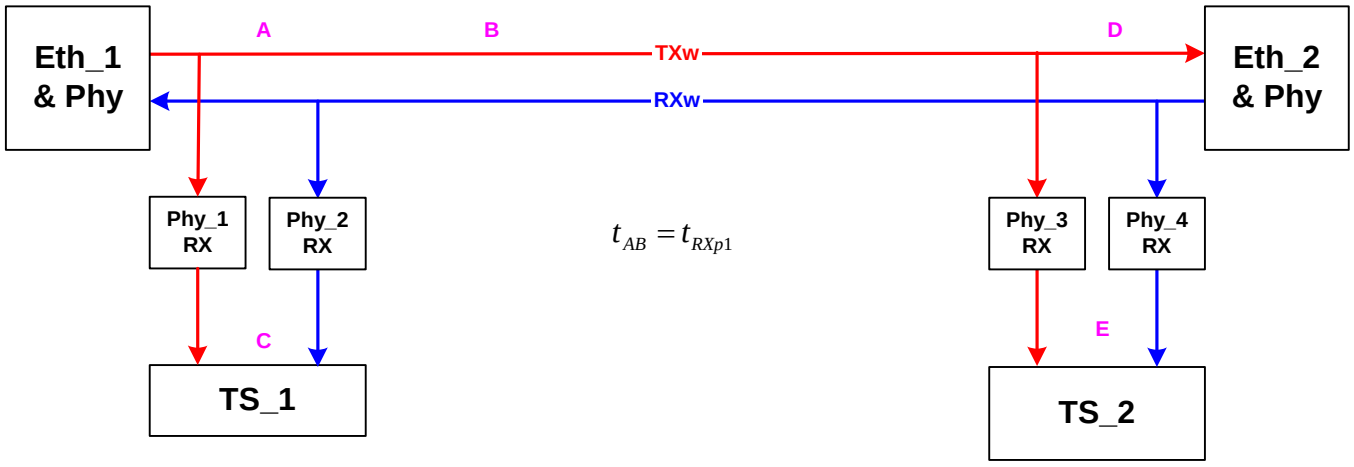
If the same PHY chips are used at in both master and slave clocks, we have

$$t_{TXp1} = t_{TXp2} \quad and \quad t_{RXp1} = t_{RXp2} \tag{5}$$

By Eqs (1) to (5), we achieve the symmetry, ie

$$t_{TX} = t_{RX} \tag{6}$$

For arch_2, we have



For one way, we have

$$t_{TX} = -t_{RXp1} + t_{TXw} + t_{RXp3} \tag{7}$$

and the other way has

$$t_{RX} = -t_{RXp4} + t_{RXw} + t_{RXp2} \tag{8}$$

Note that we're using only RX part of PHY chip. Note also that time stamps are delayed at both ends, but result in opposite effects on time stamp.

If the same PHY chips are used at in both master and slave clocks, we have

$$t_{RXpm} = t_{RXpn}, \quad m,n = 1,2,3,4 \tag{9}$$

So, Eqs (7) & (8) become

$$t_{TX} = t_{TXw} \tag{10}$$

and

$$t_{RX} = t_{RXw} \tag{11}$$

hence

$$t_{TX} = t_{RX} \tag{12}$$

therefore we also have symmetrical topology.

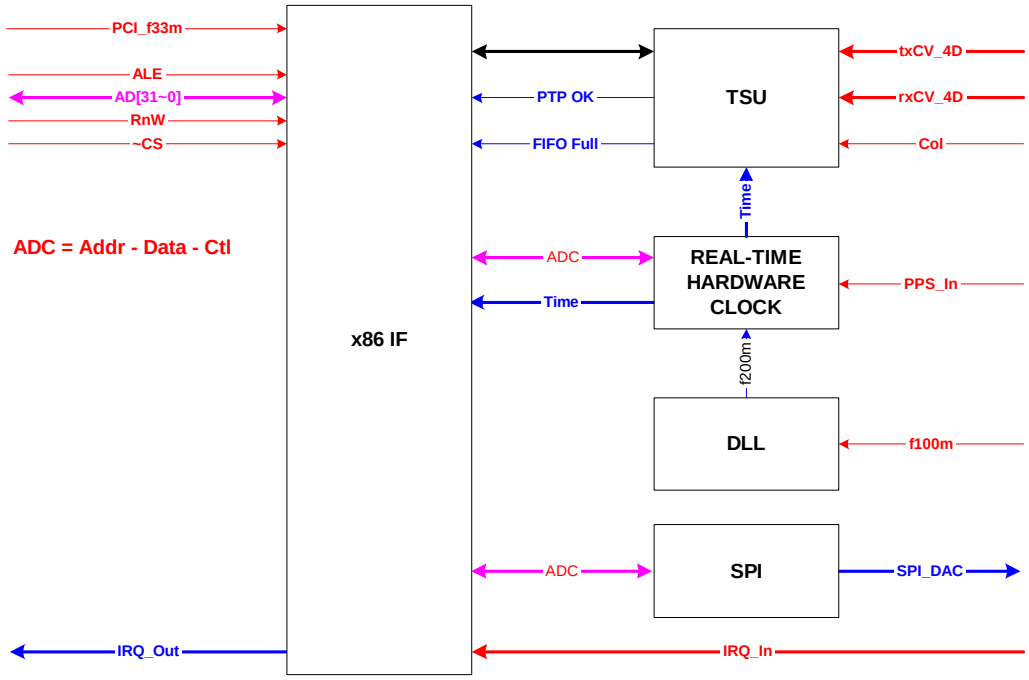
Conclusions

It doesn't matter which architecture is used, the symmetry requirement is guaranteed if we have the followings

- The same architecture is used in both master and slave clocks;
- All PHY chips in use are the *same*.

The 2nd requirement is worth further discussions. Even we use identical PHY chip, say LXT971, there are some tolerance in TX and RX due to semiconductor process. The order of this tolerance could be the same if we use different PHY chip but the same technology (5v, 3v, 2v, …).

5. FPGA Design



6. Tahiti FPGA Mem-Map

Back-Plane can access its own address space of 4 KB only, while X86 can access both BP space and its own space.

Offset	Size	Type	Description
0x0000	0x100	XLi & Local	XLi Reg
0x0100	0xC00	XLi & Local	Dual-Port RAM
0x0D00	0x100	XLi & Local	Local Reg
0x0E00	0x200	XLi & Local	Reserved (HW Debug)
0x1000	0x100	XLi* & Local	TX Reg
0x1100	0xC00	XLi* & Local	TX FIFO
0x2000	0x100	XLi* & Local	RX Reg
0x2000	0xC00	XLi* & Local	RX FIFO

XLi* : XLi requires passcode to access for HW debugging purpose.

6.1. XLi Reg Space

Offset Address	Type	Description
0x00 ~ 0x03	RO	FPGA ID
0x04 _ 0x07	RO	FPGA Version
0x08 ~ 0x0B	RO	FPGA Date Code
0x0C ~ 0x1F		*Reserved*
0x10 ~ 0x13	RO	PN High
0x14~ 0x17	RO	PN Low
0x18 ~ 0x1F		*Reserved*
0x20 ~ 0x23	RW	Control 0 : PPS_A 1 : PPS_B 3 ~ 2 : N.U. 4 : Enable Reset Minor Time
0x24 ~ 0x27	RW	Status TBD
0x28~ 0x2B	RW	IRQ TBD
0x2C ~ 0x2F		*Reserved*
0x30 ~ 0x33	RO	Major Time (Seconds)
0x34 ~ 0x37	RO	Minor Time (10 nano-Seconds)
0x38 ~ 0x3B	RO	Latched Minor Time before clear, Max expected
0x3C ~ 0x3F	RO	Latched Minor Time with clear 16 ~ 15 : at clear, 0 expected 16 ~ 31 : after clear,1 expected
0x40 ~ 0x43	RW	Set Major Time
0x44~ 0x47	RW	Reset Minor Time, clear to 0 at this value
0x48 ~ 0xFF		*Reserved*

6.2. Local Reg Space

Offset Address	Type	Description
0xD00 ~ 0xD03	RO	Major Time (Seconds)
0xD04 ~ 0xD07	RO	Minor Time (10 nano-Seconds)
0xD08 ~ 0xD0B	RO	Latched Minor Time before clear, Max expected
0xD0C ~ 0xD1F		*Reserved*
0xD20 ~ 0xD213	RW	Control 0 : 0 (Master) 1(Slave) 1 ~ 3 : Reserved 4 ~ 5 : SW LED
0xD24 ~ 0xD27		Status 0 : F100 MHz locked
0xD28 ~ 0xD2F		*Reserved*
0xD30 ~ 0Xd33	RW	IRQ Enable 0 : TX 1 : RX 2 : PPS 3 : BP
0xD34 ~ 0xD37	RW	Event 0 : TX 1 : RX 2 : PPS 3 : BP
0xD38 ~ 0xD3F	RW	IRQ Mask 0 : TX 1 : RX 2 : PPS 3 : BP

0xD40 ~ 0xD43	RW	16-bit DAC
0xD44 ~ 0xCFF		*Reserved*

6.3. PTP Reg Space (TX / RX)

Offset Address	Type	Description
0x00 ~ 0x03	WO	Update FIFO for 1 PTP pkt (8 32-bit long word)
0x04 _ 0x07	RO	FIFO Status 9 ~ 0 : Number of FIFO Item (long word, inc. by 8 for 1 packet) 23 ~ 10 : N.U. 24 : FIFO Empty 27 ~ 25 : N.U. 28 : FIFO Full
0x08 ~ 0x0B	RO	9 ~ 0 : Number of long word written into FIFO
0x0C ~ 0x0F	RO	9 ~ 0 : Number of long word read out of FIFO
0x14 ~ 0x1F		*Reserved*
0x20 ~ 0x23	RW	Control TBD
0x24 ~ 0x27	RW	Status TBD
0x28 ~ 0xFB		*Reserved*
0xFC	WO	Reset FIFO pointer (Rd / Wr), not the content

7. Getting Start

After powered up, the unit is in slave mode (0xD20-0 = 1)

Master Mode

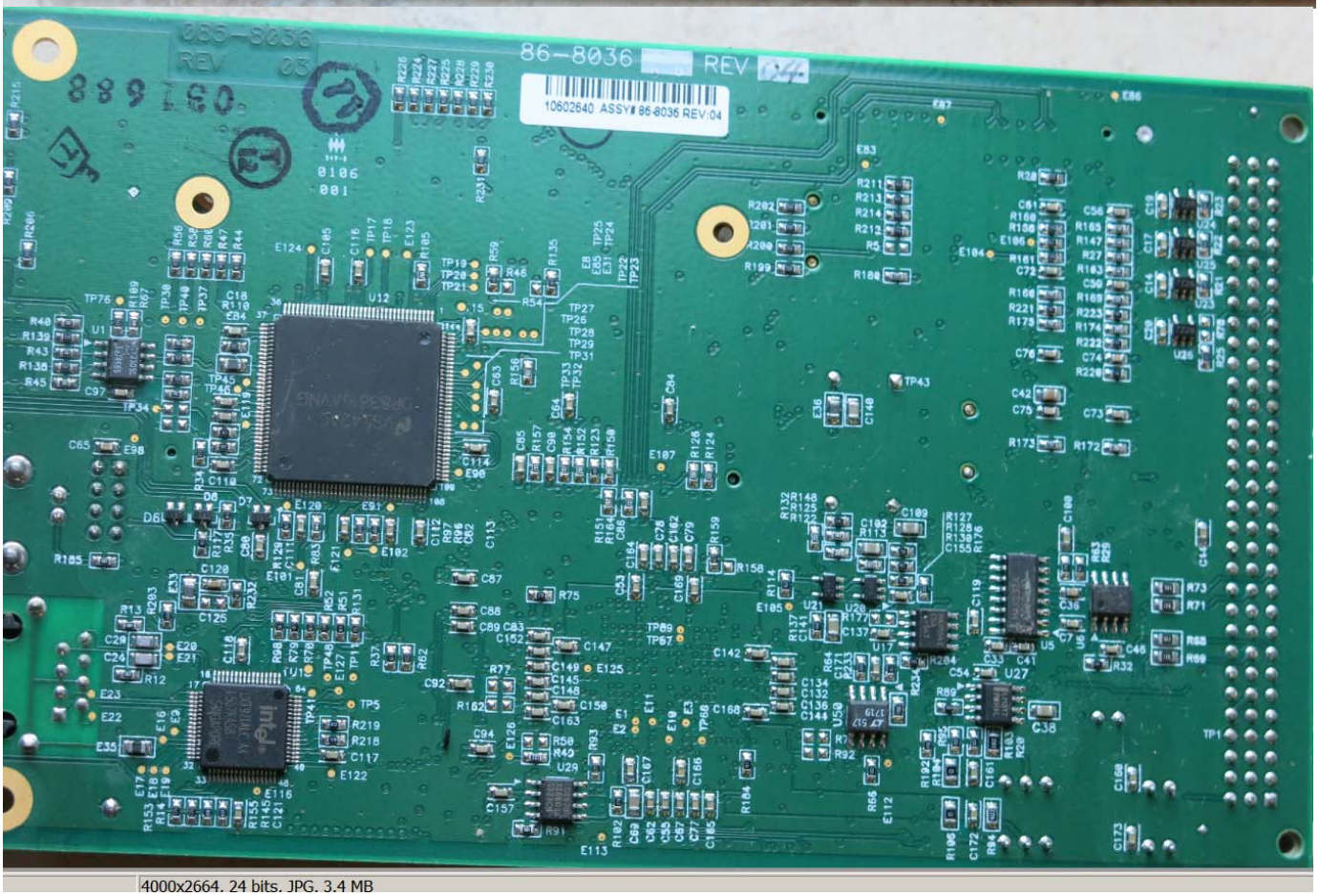
Clear 0xD20.0 = 0
Set Major Time 0x3C
Check TX FIFO 0x1100

Start PTP application SW

Slave Mode

Set 0xD20-0 = 1 for slave mode
Set 0x20-4 = 1 to enable Reset Minor Time

Set 0x40 to jam Minor Time
Set 0xD40 for DAC / VCO (PLL)



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