Treadstone HW Architecture

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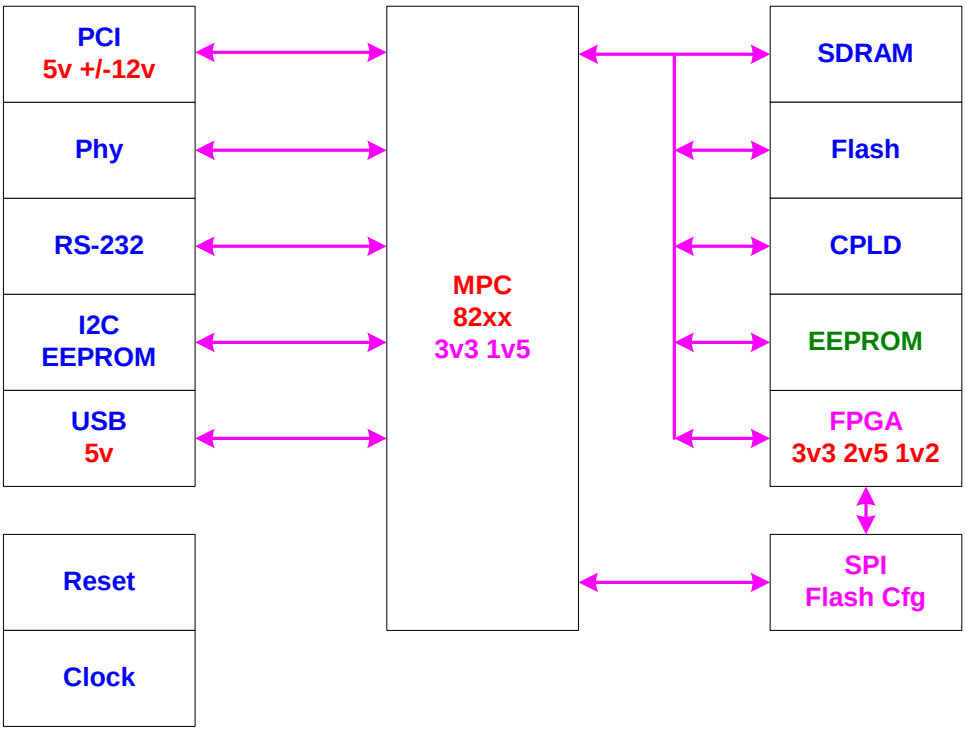
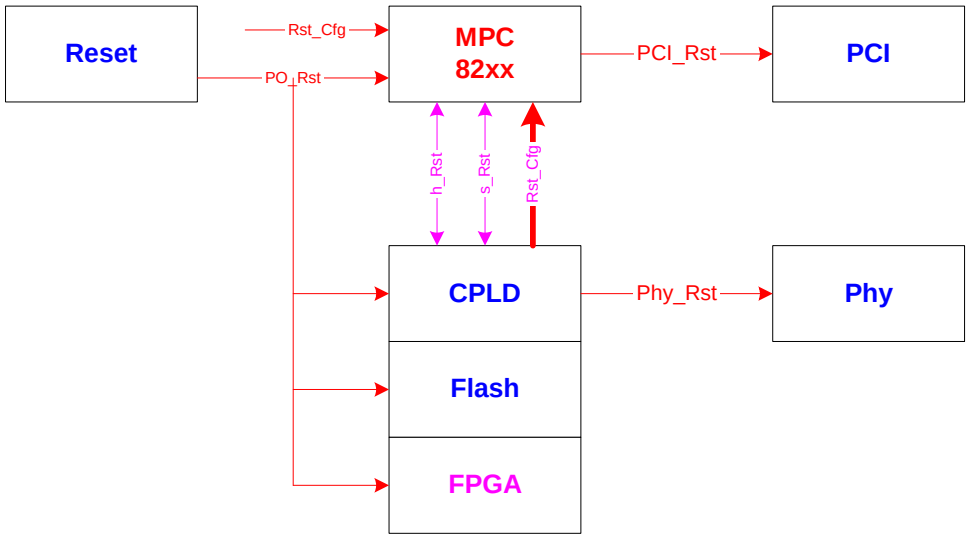
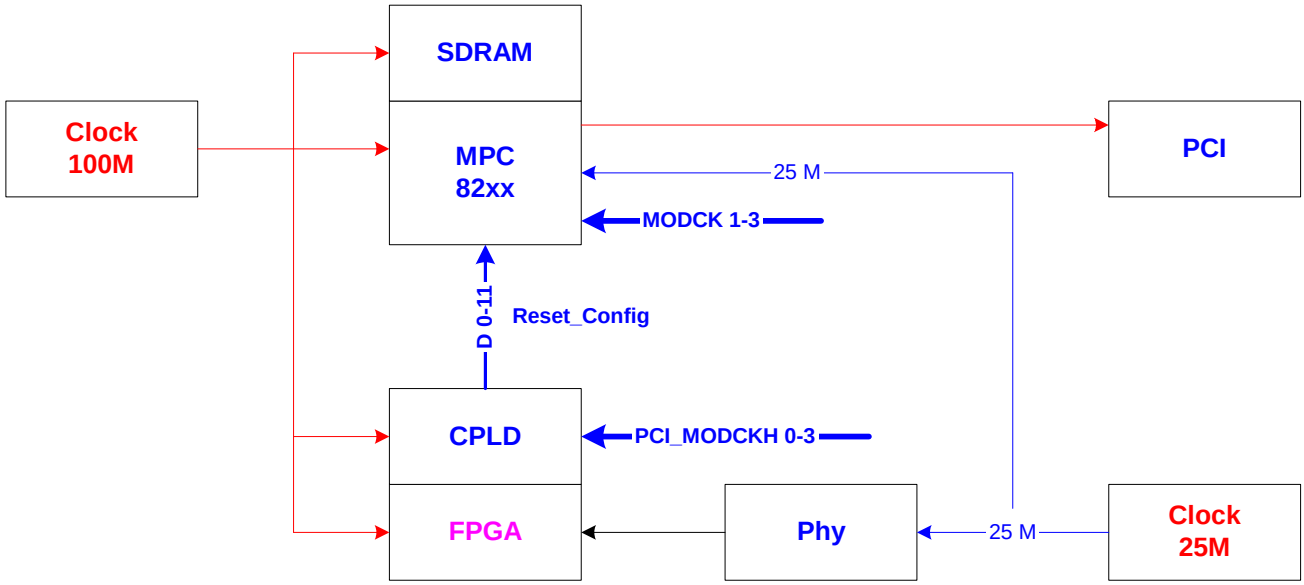
1. OverView

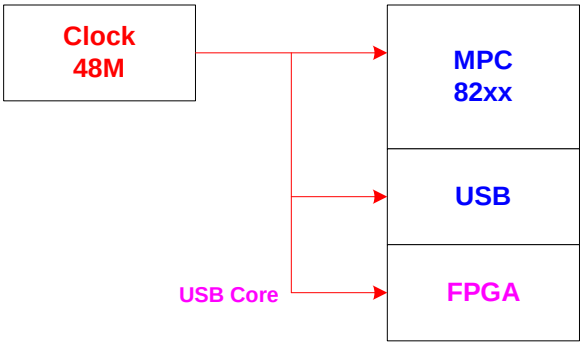


2. Reset

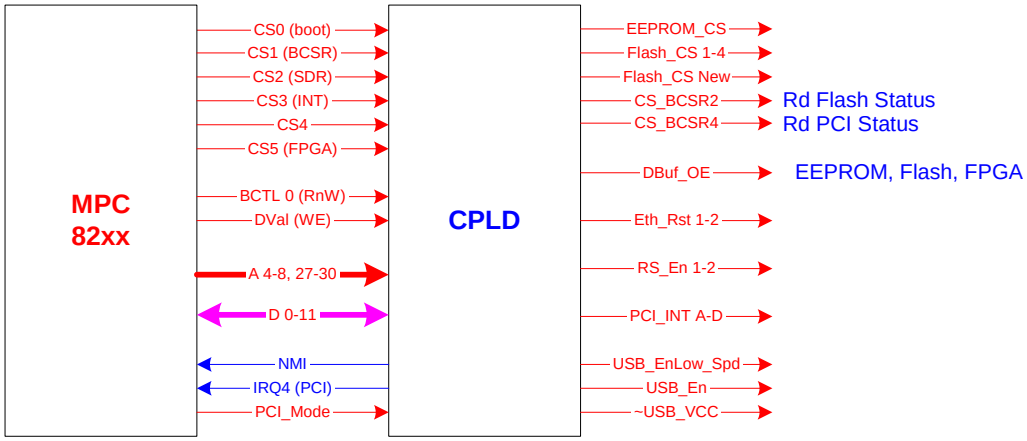


3. Clock





4. CPLD



The two possible configuration words are the following:

- FLASH/BCSR is the boot device. CS0 is assigned to the FLASH and CS4 is assigned to the E^2PROM.
- E^2PROM is the boot device. CS0 is assigned to the E^2PROM and CS4 is assigned to the FLASH.

Table 5-5. MPC8272ADS Chip Select Assignments

Chip Select:	Assignment	Bus	Timing Machine
CS0	Flash SIMM / E^2PROM [1]	60X (Buffered)	GPCM
CS1	BCSR	60X (Buffered)	GPCM
CS2	SDRAM	60X (Main)	SDRAM Machine 1
CS3	PCI Interrupt Controller	60X (Buffered)	GPCM
CS4	E^2PROM / Flash SIMM[a]	60X (Buffered)	GPCM
CS5	ATM UNI Microprocessor I/F	60X (Main)	GPCM
CS6	Communication Tool M/P Interface CS1.	60X (Buffered)	GPCM/UPMx
CS7	Communication Tool M/P Interface CS2.	60X (Buffered)	GPCM/UPMx

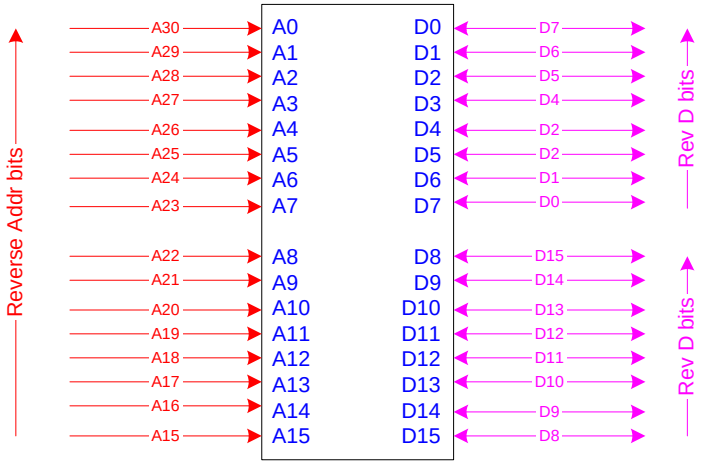
[1] Selection is done by a dip-switch.

5. Bit Order

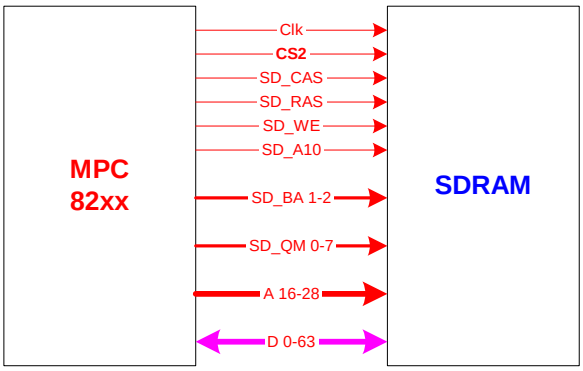
PowerPC supports both big and little endians in case multi-byte access. High byte goes to high address in big endian but goes to low address in little endian.

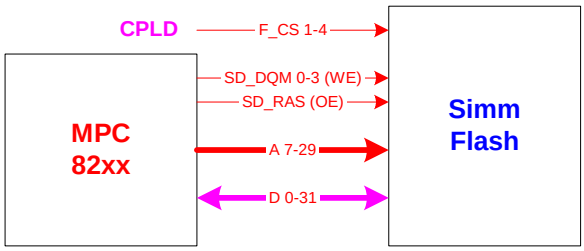
Endian is about byte order. In addition, PowerPC has reverse bit order. Normally, we're dealling with A[31..0] and D[15..0]. Now we're working with A[0..31] and D[0..15].

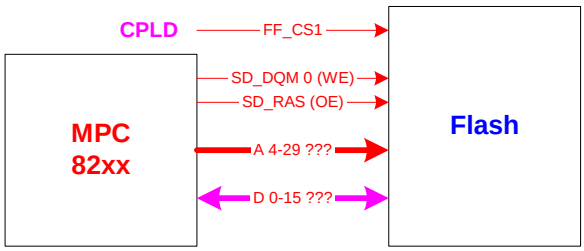
For PowerPC, we have to reverse address bit. For data bit, we may not want reverse data bit in accessing RAM as we'll find no difference at all if we write into some order and read in exactly the same order. However, if we need to read some chip ID, we have take bit order into account. Note that if we want byte access, we have to reverse data bit order on byte boudary.

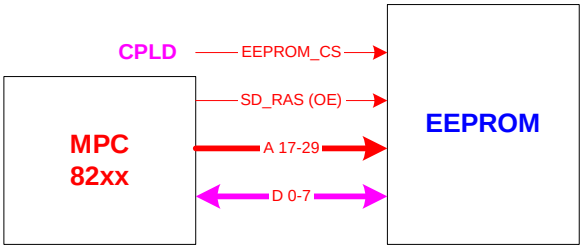


6. System Bus









BCSR2_CS : {SWOPT[0-1], ‘b00},
{BVER[1-0], BREV[1-0]},
{SWOPT2, F_PD[7-5]},
{F_PD[4-1]}

BCSR4_CS : {PCI_PRSNT0[1-2], PRSNT1[1-2]}
{2’b0, PCI_M66EN, 1’b0}

CPLD -> DBUF_EN : DAT[0-15] -> BDAT[0-15]

7. SPI Flash

Requirements:

- Xilinx is configured by SPI flash. In normal opertion, board reset drives PROG_B low, hence CS_B low to start configuring FPGA from SPI flash;
- Xilinx is also configured by PC via JTAG in case failure with SPI flash, 4 resistors of 0 Ohm must be loaded to do this job;
- SPI flash is programmed by uP SPI, an extra GPIO pin of PPC is used to activate Z buf and drive PROG to zero for tristating FPGA. In normal operation, this Z buf is in Z-state;
- SPI flash is also programmed by PC in case failure of uP SPI (either code unavailable, or something else); a jumper is required to drive PROG to zero for Z-stating FPGA.

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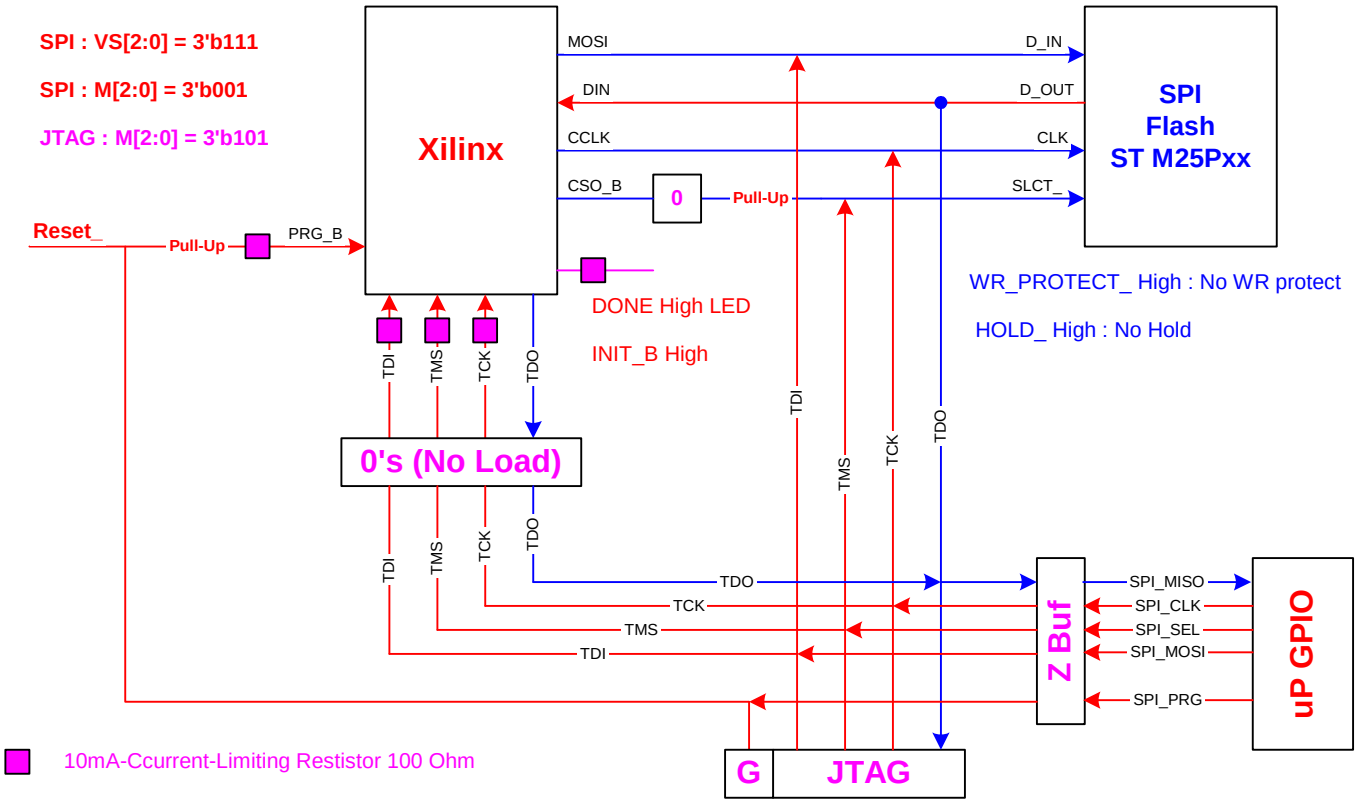
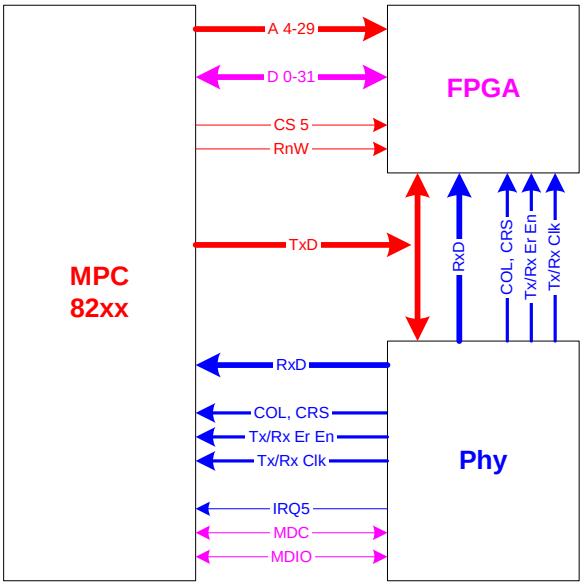
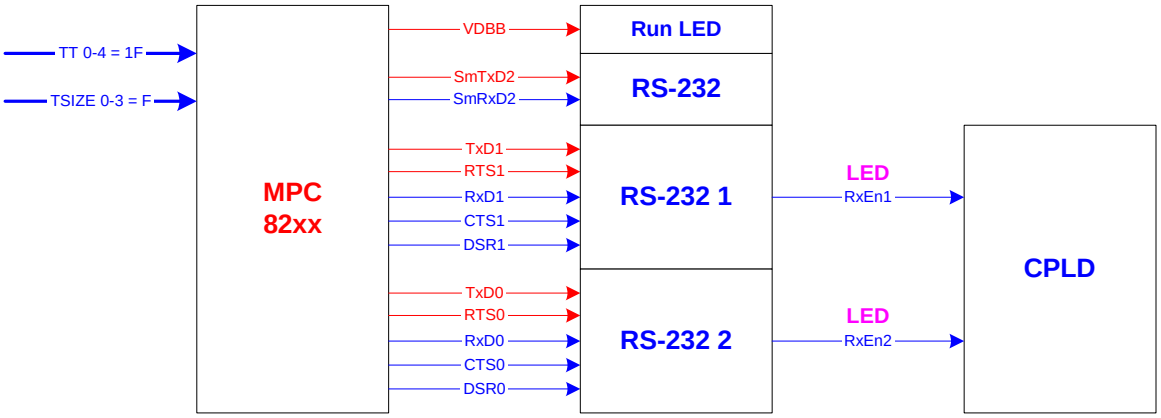


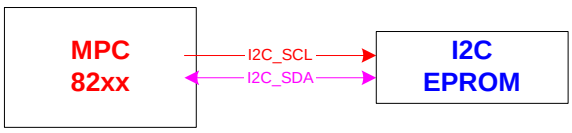
8. FPGA



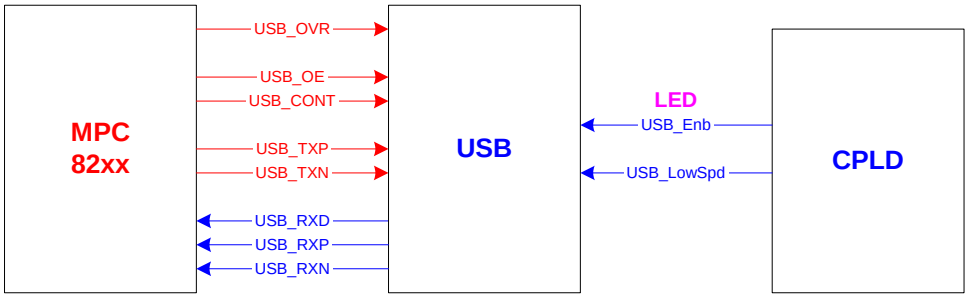
9. Peripheral



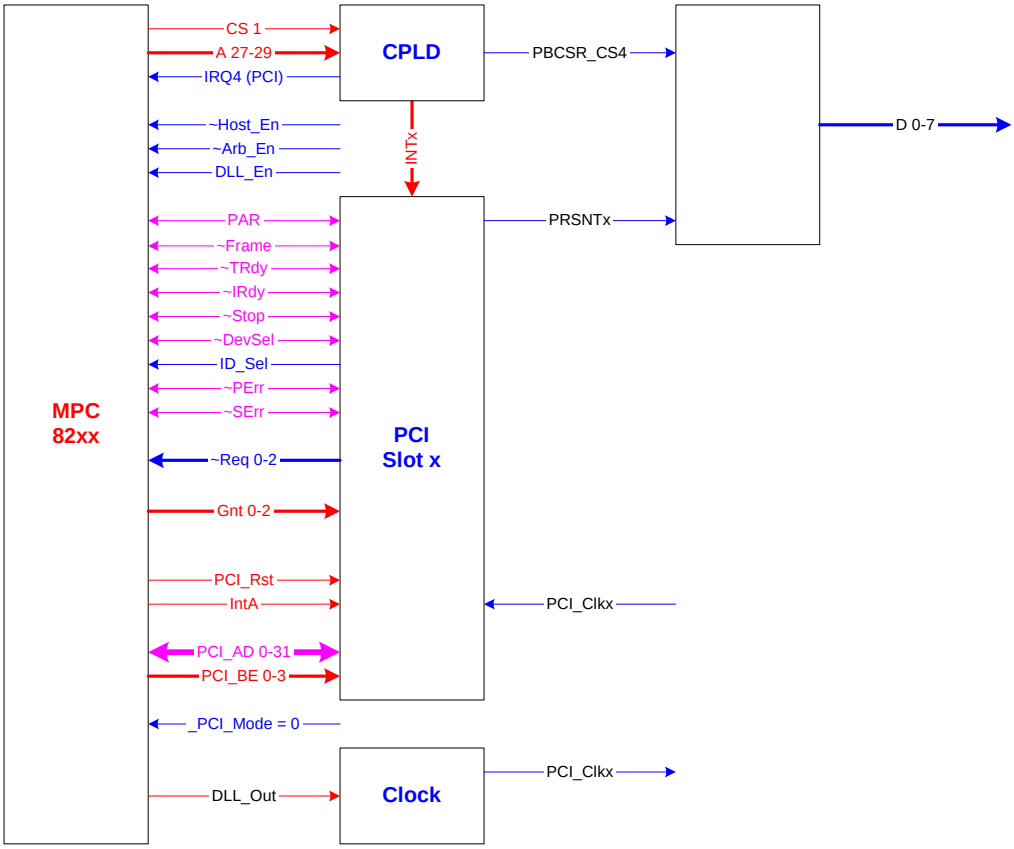
10. Serial Storage



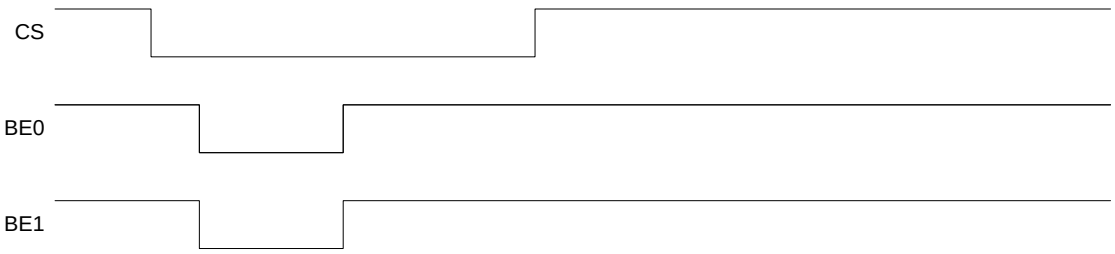
11. USB

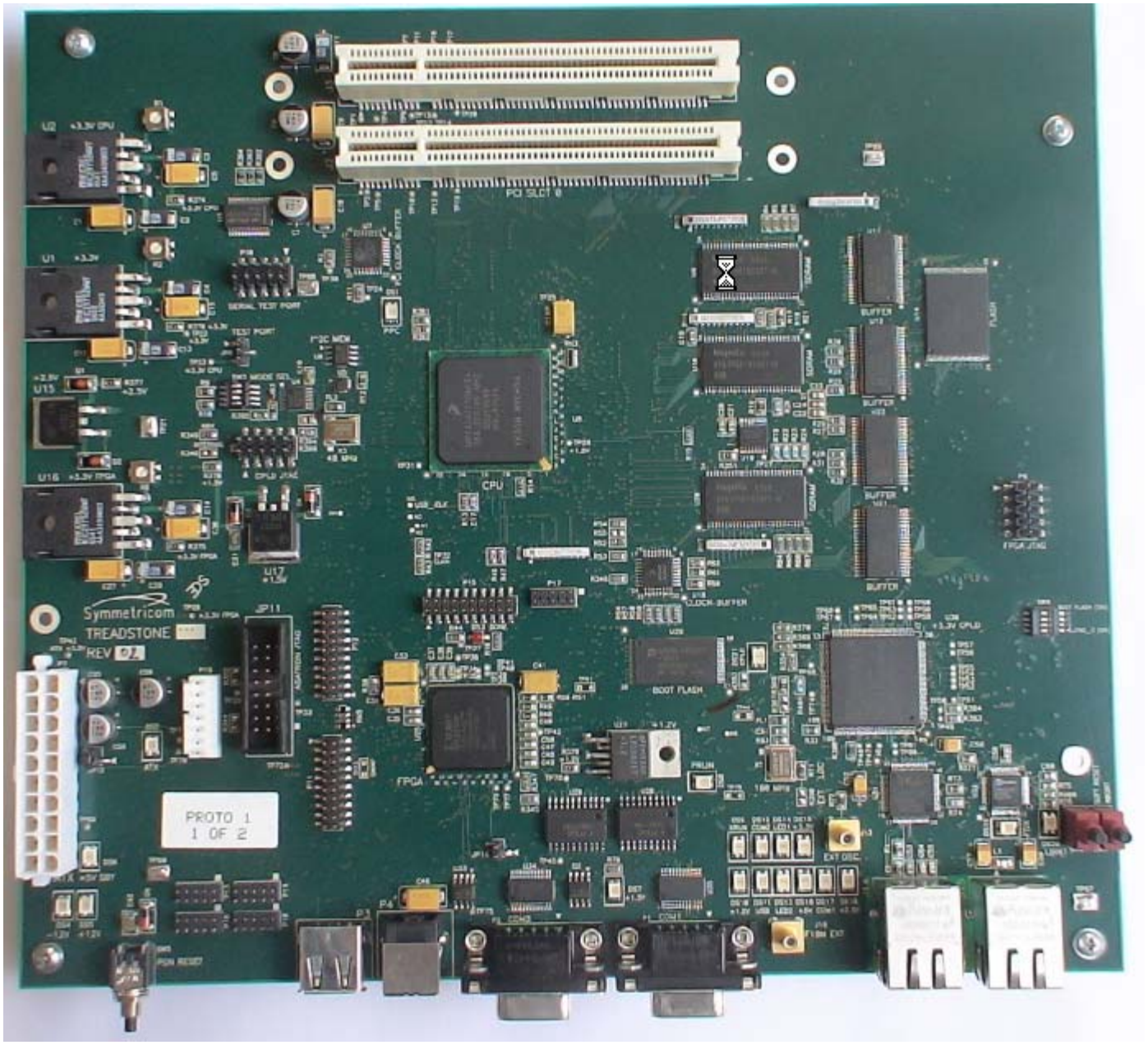

MPC
82xx
USB_OVR
USB_OE
USB_CONT
USB_TXP
USB_TXN
USB_RXD
USB_RXP
USB_RXN
USB
LED
USB_Enb
USB_LowSpd
CPLD

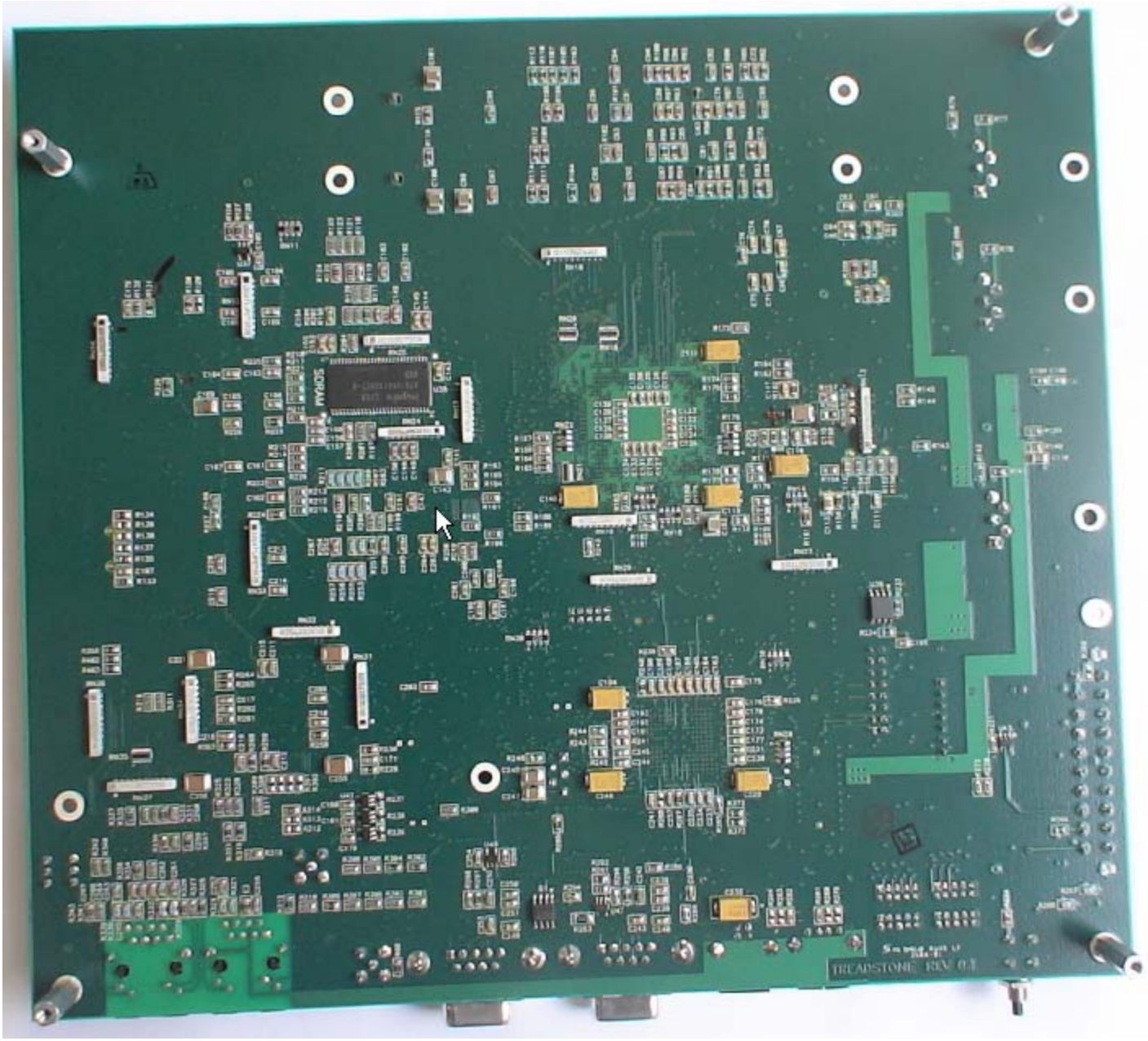
12. PCI


MPC
82xx
CS 1
A 27-29
IRQ4 (PCI)
~Host_En
~Arb_En
DLL_En
PAR
~Frame
~TRdy
~IRdy
~Stop
~DevSel
ID_Sel
~PErr
~SErr
~Req 0-2
Gnt 0-2
PCI_Rst
IntA
PCI_AD 0-31
PCI_BE 0-3
_PCI_Mode = 0
DLL_Out
CPLD
INTx
PCI
Slot x
Clock
PBCSR_CS4
PRSNTx
PCI_Clkx
PCI_Clkx
D 0-7

13. Bus Timing




Symmetricom
TREADSTONE
REV 02
PROTO 1
1 OF 2
PCI SLOT 0
CPU
FPGA
BOOT FLASH


TREADSTONE REV 0.1